PERIPHERAL EXPANSION SYSTEM

Theory Of Operation And Technical Training Manual

UPDATE TRACKS

07/13/82

* Corrected VDP and GROM addresses.

09/03/82

* Updated pinouts to include Second Generation CPU bits.

TI 99/4 PERIPHERAL EXPANSION
TECHNICAL TRAINING COURSE OUTLINE

This outline will serve the repair technician both as a guide to the portions of the Peripheral Expansion System Theory of Operation which are applicable as service information, and as a syllabus for a series of peripheral repair training sessions. The apparent breaks in consecutive numbering are due to planned omission of subjects not related to repair. The Theory of Operation, however, will be provided unedited since some individuals may be interested in system design considerations as an extra-curricular activity.

It is recommended that review of this theory of operation be accomplished along with a detailed study of the applicable system schematics.

SECTION 1

CPU REQUIREMENTS

1.1 GENERAL COMMENTS

The purpose of these notes is to outline considerations necessary or advisable for hardware interfacing peripherals to the 99/4. If this interface is to be through the Peripheral Expansion Unit the rules become more complex due to the fact that two different processors may be used to drive the PEU. It will obviously be to TI's advantage if the involved peripheral will function correctly with both processors. To make matters worse, the timing of the second generation processor has not been published. I think I can safely say that ROM and SRAM based designs will work with either case, but designers of DRAM based logic beware!

Required 99/4 timing is shown in the TI 99/4 TECHNICAL DATA manual, and another separate document is available to detail the Software requirements for peripheral interfacing.

1.2 99/4 MEMORY SPACE ORGANIZATION

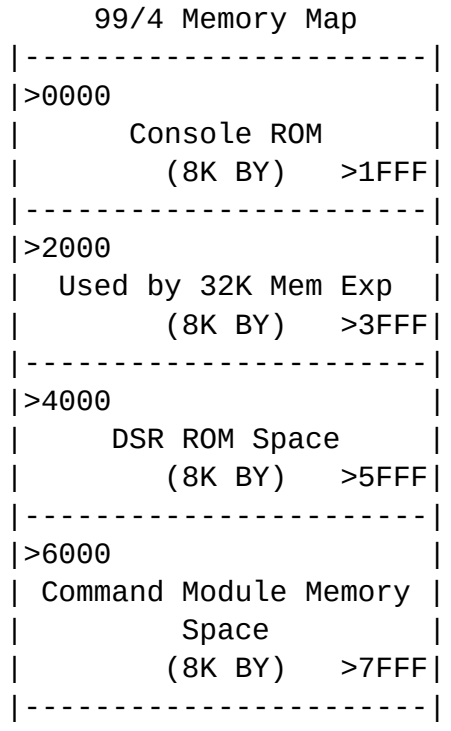
The memory map of the TI 99/4 is as follows. The allocated spaces are shown in parentheses, and the actual memory space used is shown where applicable. This is notable of the Memory Mapped Devices (MMD) in the >8000 to >9FFF space. All of these devices live in 1K blocks, and block decoding is used to select them. Even though they are shown to respond at their base address, they will respond ANYWHERE in the 1K block assigned to them. This is certainly true of the 128 BYTE SRAM which is decoded to respond at a base of >8000 but it is noted in the literature to respond at a base of >8300. Software is written to conform to the letter base. The point I am trying to make is that there is a given amount of wasted space, BUT YOU CANNOT TAKE ADVANTAGE OF IT BECAUSE OF THE BASIC SPACE DEFINITION AND THE DECODING USED ON EXISTING PRODUCTS.

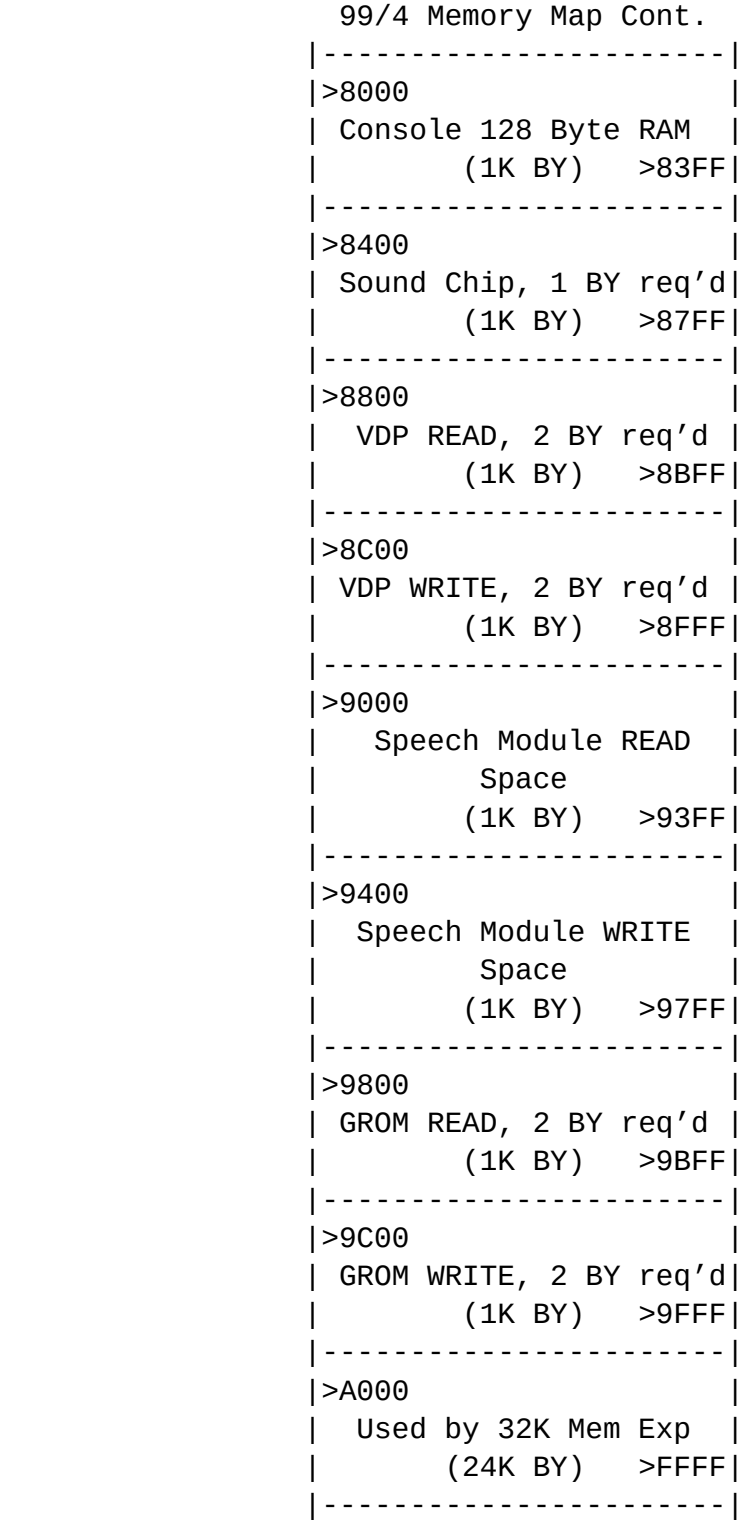
1.2.1 READ before WRITE Considerations. Note also that there are different READ and WRITE addresses for most of the MMDs.

This is because the TMS9900 does a READ operation at the destination address prior to writing to it. GROMs in the MMUs have internal address registers that autoincrement after either a READ or a WRITE operation and this GROM characteristic, if unchecked, rarely produces the desired results.

The READ before WRITE exists because the GROM is a WORD oriented machine from a memory access standpoint. The several BYTE oriented instructions are carried out by the machine in a WORD world, and the other BYTE in the WORD must not be altered. The machine itself must save the unaltered BYTE, concatenate the new BYTE with it, and then return the WORD to memory. The internal logic of the TMS9900 is such that it was to the designer’s distinct advantage to do this same READ before WRITE on both BYTE and WORD moves. While this is an easy design fix, it certainly is nice to know the problem exists prior to any design efforts.

1.2.2 Command Module Memory Space. The Command Module Memory Space must be treated as logically connected to the Command Module Port only. The GROM chips are rather poor line drivers at best, and their life on the I/O Data Bus is limited. Even though the GROM Data Bus is connected directly to the I/O Data Bus currently, there is no guarantee that updated versions of the 99/4 will have the same connection. I think one can safely say that new generation products will isolate the GROM Data Bus from the I/O Data Bus. DON’T TRY TO ACCESS THE COMMAND MODULE MEMORY SPACE FROM THE I/O PORT.


99/4 Memory Map
>0000
Console ROM
(8K BY) >1FFF
>2000
Used by 32K Mem Exp
(8K BY) >3FFF
>4000
DSR ROM Space
(8K BY) >5FFF
>6000
Command Module Memory
Space
(8K BY) >7FFF



1.3 CRU SPACE DEFINITION

As it is with the Memory Space decoding the 1K space devices are not fully decoded. Thus, most devices will respond just as well to other addresses in their block as they will to the block base address.

By and large the CRU space is allocated to peripherals with only a very small amount devoted to internal mapping control (Keyboard Scan, Cassette control, etc.).

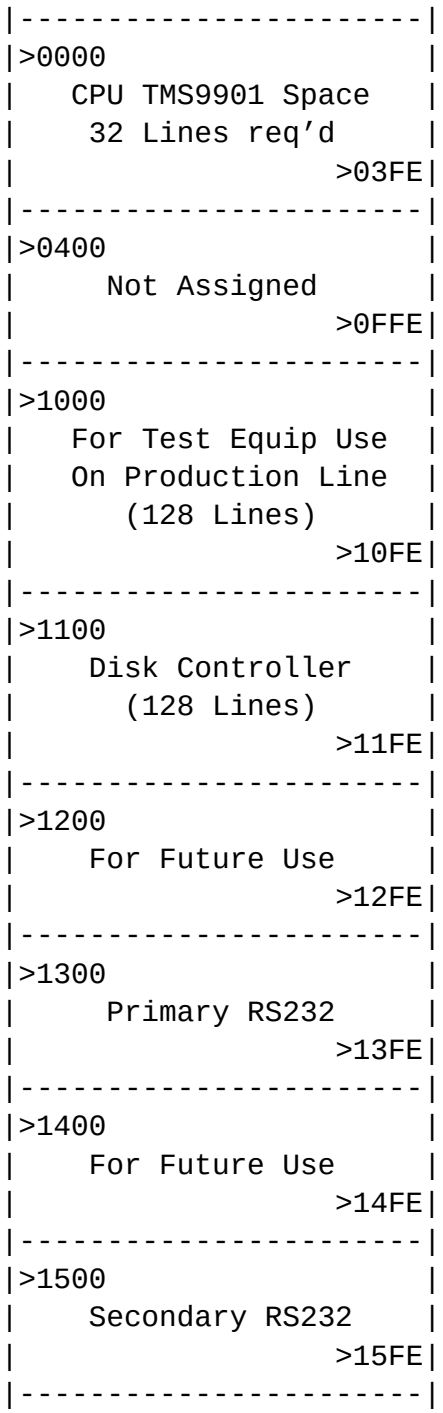
1.3.1 Disallowed Instructions. The CRU control input “CRUCLK” is also not fully decoded, and as the result of not including the most significant three Address Bus bits in the strobe, certain instructions of the TMS9900 must be disallowed. These are LREX, CKOF, CKON, RSET, and IDLE. ONE MUST NOT USE THESE INSTRUCTIONS, AS THE LOGIC BLOCKS FED BY CRUCLK WILL THINK THAT STROBE IS FOR A CRU OPERATION.

1.3.2 CRU Output Definition. There is only one restriction on the definition of CRU output bits for Peripheral use, and that is the base address bit. It must be used to read in DSR ROMs when SET and should where possible be RESET by the POWER ON RESET line in the I/O Port. Thus, the DSR ROM will be paged out by a RESET operation. For more information, see the paragraph on DSR ROM Considerations.

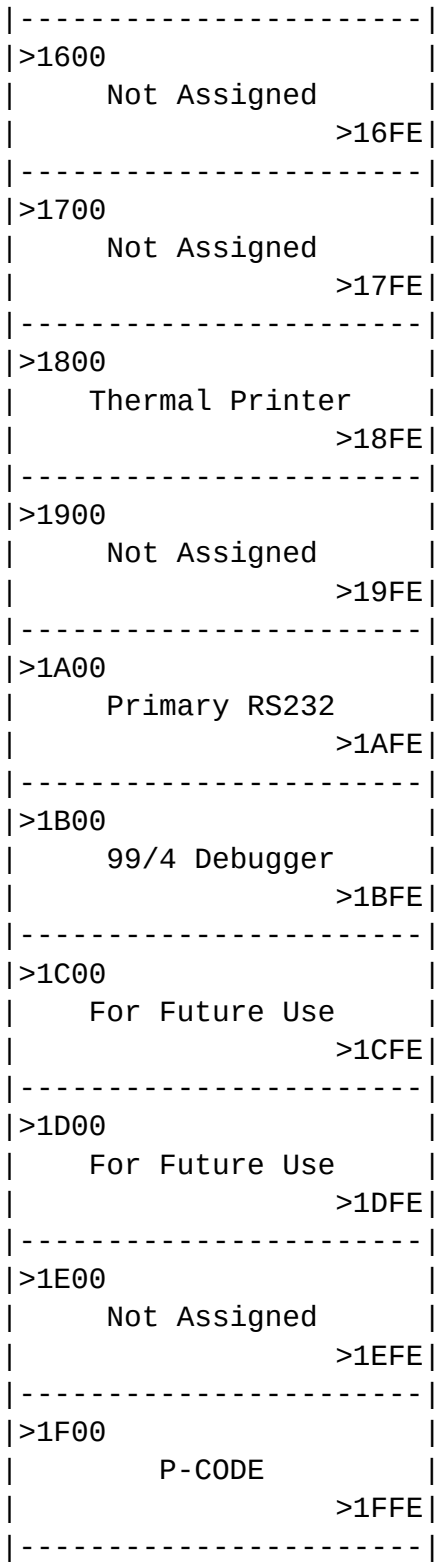
1.3.3 CRU Input Definition. There is no definition for CRU input lines, and one is free to define them within that Peripheral Space as desired.

1.3.4 Spare CRU Bit Use. Spare CRU bits may be put to good use as test bits. If spare INPUT and OUTPUT bits are available, the ones used should be chosen such that spare INPUTs may be connected to spare OUTPUTs, each pair displaced by the same amount from the base to form software FLAG Bits. Otherwise, spare inputs should be tied to VCC and GROUND in some manner that will be verified during the power up routine execution for that peripheral. Spare outputs may be left unconnected or terminated on an etch pad to be connected to Automatic Test Equipment.

CRU Map


>0000
CPU TMS9901 Space
32 Lines req'd
>03FE
>0400
Not Assigned
>0FFE
>1000
For Test Equip Use
On Production Line
(128 Lines)
>10FE
>1100
Disk Controller
(128 Lines)
>11FE
>1200
For Future Use
>12FE
>1300
Primary RS232
>13FE
>1400
For Future Use
>14FE
>1500
Secondary RS232
>15FE

CRU Map, Continued



1.4 99/4 PERIPHERAL POLLING

The 99/4 polls the I/O Port for the presence of peripherals on either a Software Restart or a Hardware RESET. This polling starts in the CRU Space at >1000, and continues in >100 increments until >1F00 has been polled. Power up routines will be executed for each peripheral as its DSR ROM is polled (if the DSR header indicates that a power up sequence is required).

1.5 INDICATOR LED

An Indicator LED shall be provided, and shall be driven by a unique CRU OUTPUT bit. If all CRU OUTPUT bits have been defined, it shall be acceptable to connect the LED drive to the DSR ROM Page Bit.

1.6 DSR ROM CONSIDERATIONS

The DSR ROMs for all peripherals must be placed at >4000 and may be contiguous through >5FFF. These ROMs must not respond unless the respective CRU DSR ROM Page Bit is set ON (SET to a HIGH level with either a SBO instruction or “1” data in a LDCR instruction). It is the responsibility of the CPU to insure the proper control of all of the DSR ROM Page Bits.

1.6.1 Extended DSR ROM Techniques.

ROM Space in excess of 8K BYTES may be obtained by paging the paged DSR ROM. This secondary paging may be used anywhere in the 99/4 Memory Space, and has been used in both the Command Module Space and in the DSR ROM Space. The Secondary Page Bit may be obtained easily from the assigned CRU space to that Peripheral (as was done on the P-CODE PCB) or by WRITING to a ROM Address and then decoding that condition to strobe a Flip-Flop. The latter method was used on the Extended BASIC Command Module to page the upper 4K half of that space. Either a Data Bus or an Address Bus bit may be used for data to the FF. Both schemes provided a non paged 4K base ROM, and paged the upper 4K half of the space.

SECTION 2

EXPANSION BOX REQUIREMENTS

2.1 System Bus Requirements

There are only two design considerations to be comprehended in interfacing to the system bus. One controls a Data Bus driver on the 99/4 end of the connecting cable, and the other is used during PCB Burn In.

2.1.1 Remote Data Bus Driver. As has been previously noted, there are additional requirements for interfacing through the Peripheral Expansion Unit. Regardless of the processor driving the PEU, a signal must be provided to indicate to the interface that a memory cycle is being requested for a PCB in the PEU. This signal is termed “RDBENA*”, and is used to enable Data Bus drivers on the 99/4 end of the cable. It must function as an open-collector signal, and be LOW True for the full memory cycle on that PCB. I have used the same signal that drives my bidirectional Data Bus driver chip for the enable on a tri-state gate (with its input connected LOW) in the past for this function.

2.1.2 Burn In Consideration. A single HIGH True line shall be provided to enable the PCB to respond to both Memory and CRU accesses. This line is held at a HIGH level in the PEU, but is driven to allow a parallel connection of 8 PCBs during Burn In. When LOW, this signal shall disable the PCB from driving any of the System Memory and CRU Bus lines. I have excepted the interrupt sensing from this in the past.

2.2 POWER ALLOCATION ASSUMPTIONS

The following is a guide for maximum load current a PCB should present to the PEU.

* 250 ma on the +15V unregulated bus.

* 500 ma on the +8V unregulated bus.

* 30 ma on the -15V unregulated bus.

2.3 SYSTEM BUS PIN DEFINITION

.100” PIN TO PIN SPACING, ATTLEBORO CONNECTOR

PIN #	MNEMONIC	FUNCTION
1		+5V 3-T Regulator supply voltage
2		+5V 3-T Regulator supply voltage
3	GND	Logic Ground
4	READY.A	System READY
5	GND	Logic Ground
6	RESET*	Active LOW System driven RESET
7	GND	Logic Ground
8	SCLK	System Clock
9	LCP	Second Generation CPU indicator. 0=Second Gen CPU, 1=99/4
10	AUDIO	Input Audio
11	RDBENA*	Active LOW Remote Data Bus Driver Enable control line
12	PCBEN	Active HIGH PCB enable for Burn In
13	HOLD*	Active LOW CPU HOLD request Second Generation CPU only
14	IAQHDA	IAQ HOLDA Logical OR Second Generation CPU only
15	SENILA*	Interrupt Level A Sense Enable
16	SENILB*	Interrupt Level B Sense Enable Second Generation CPU only
17	INTA*	Active LOW Interrupt Level A
18	LINSP	LOW for 99/4 Memory Expansion, HIGH for linear memory space. Second Generation CPU only
19	D7	System DATA Bus, LSB
20	GND	Logic Ground
21	D5	System DATA Bus
22	D6	System DATA Bus
23	D3	System DATA Bus
24	D4	System DATA Bus
25	D1	System DATA Bus
26	D2	System DATA Bus
27	GND	Logic Ground
28	D0	System DATA Bus, MSB
29	A14.A	Address Bit
30	A15/COUT.A	Address Bit, LSB
31	A12.A	Address Bit
32	A13.A	Address Bit
33	A10.A	Address Bit

SYSTEM BUS PIN DEFINITION, CONTINUED

PIN #	MNEMONIC	FUNCTION
34	A11.A	Address Bit
35	A08.A	Address Bit
36	A09.A	Address Bit
37	A06.A	Address Bit
38	A07.A	Address Bit
39	A04.A	Address Bit
40	A05.A	Address Bit
41	A02.A	Address Bit
42	A03.A	Address Bit
43	A00.A	Address Bit
44	A01.A	Address Bit
45	AMB.A	Address Bit, normally HIGH
46	AMA.A	Address Bit, normally HIGH
47	GND	Logic Ground
48	AMC.A	Address Bit, MSB normally HIGH
49	GND	Logic Ground
50	CLKOUT*	Active LOW CPU Clock
51	CRUCLK.A*	Active LOW CRU Output Clock
52	DBIN.A	Data bus Dir’tn HIGH is CPU READ
53	GND	Logic Ground
54	WE.A*	LOW true CPU Write Enable
55	CRUIN	HIGH true CRU Input Data
56	MEMEN.A*	Active LOW memory request
57		-12V 3-T Regulator supply voltage
58		-12V 3-T Regulator supply voltage
59		+12V 3-T Regulator supply voltage
60		+12V 3-T Regulator supply voltage

SECTION 3

GENERAL HARDWARE REQUIREMENTS

3.1 PURPOSE

The purpose of this Section is to provide some insight on the hardware interface to the 99/4A via the Expansion box, and how to bring a design into production.

The actual product hardware design time represents between 1/20 and 1/5 the time necessary to bring a product into production. The vast majority of the time involved will be in doing in essence “dog work”. A detailed test specification must be written, a detailed Trouble Shoot and Repair manual must be written, the product must be Qualified by a CPG QA, Assembly Tooling must be defined, etc. Thus, there are many more tasks to be handled past the design. If these details are not handled (as they have not been on several notable products), great time demands, misunderstandings, and other bad things will be rained all over the designer. The end result is many more man hours spent than necessary.

As a design aid the Peripheral Computer Group has two prototyping PCBs, one to drive the System Bus, and one to receive that Bus. These PCBs will accommodate about 36 16-pin DIP sockets, and have the necessary System Bus buffers in place with etch connections to the System I/O pins. The PCB designers need only to hook the buffered world into theirs. Other design rules are included elsewhere in this Section. Schematics of these PCBs are available, and standard 99/4A timing diagrams should be used for the PEU PCB Design. Timing Diagrams for the next generation HC products will be included as they are published.

3.2 TESTING

Signature Analysis has been selected as primary method for TS&R of the PCBs. Hewlett Packard reps will be happy to present a short seminar on this if an individual has no prior knowledge of SA. Pattern generators will be designed for known 99/4 products, and details of these will be made available when they have been completed. We will try to design these test systems in

the general sense to provide some coverage of currently undefined products.

We observe the design rules of double spacing non +5V power (+12V, -5V, and -12V) to minimize a TTL to power line short or a power etch to power etch short. This should be a requirement for your PCB design team also.

3.3 DESIGN RULES

This paragraph covers both Hardware and PCB design rules.

* Each PCB must be completely disabled by an Active LOW disable (Active HIGH enable). The disable must disable both Memory and CRU functions on the PCB, and is used for Burn In purposes.

* The +12V, -5V, and -12V power etches shall be double spaced from other etches where possible, thus TTL damaging shorts are minimized.

* Signals such as CRUIN that are taken very far from the System I/O connector shall be guarded with GROUND etch. Where practical, these signals should be buffered with tri-state buffers.

* Buffers to drive the bus must be physically close to the I/O Bus. The prototyping PCBs have most of this already in place, but signals such as READY and CRUIN do not have them as they are not always used. A connection to the System Bus constitutes a stub connection, and generally obeys transmission line theory. These stubs should be kept as short as is practical.

* All 19 System Address bits shall be included in the Memory Space decode for that peripheral. Assume AMC, AMB, and AMA to be in the HIGH state.

* Address lines A00 through A07 shall be included in the CRU Space decode even though the 99/4 assumes A00 thru A02 to be zero.

* There are two levels on which to interrupt but the 99/4 supports only one (INTA*). THIS IS THE ONE YOU MUST USE. Interrupt level status bits are defined by the Personal Computer PCC at TI, and for the moment not sensed by the 99/4. If they were to be sensed, the 99/4 would cause a

line to go LOW (SENILA*) which tells the PCB Logic to gate its status bit to the System Data Bus.

SECTION 4

RS-232 PCB, 99/4B, AND JOHNNY BOX

SPEC DWG. #0000005

02/05/82

UPDATE TRACKS

7/21/81

* Changed Parallel I/O Port pin definition in hopes of using a commercially available cable.

* Added user jumper to +5V on Parallel I/O Port.

* Added CRU bit definitions.

7/22/81

* Added new System I/O Pin definitions to reflect new address bit, and the new .1" pin to pin spacing.

* Redefined Parallel I/O Pinouts because of lack of space on I/O tab for the 26-pin connector.

7/28/81

* Found and corrected references to "two MSB Address Lines" to "three MSB Address Lines".

8/17/81

* Added Mnemonic definition list.

* Reworded Parallel I/O Port definition to state an address bias for the CRU handshake lines.

8/18/81

* Added paragraph on 99/4A to 99/4B Software incompatibility.

8/19/81

* Changed PIO Port configuration bit to be "1" for the INPUT mode.

* Changed PIO Port handshake address bias to 4, and the configuration address bias to 2.

8/20/81

* Added paragraph on 99/4A/B sense bits.

* Added paragraph on the Indicator LED.

10/01/81

* Tried once again to define 4A/4B DSR ROM compatibility. There is none.

11/13/81

* Started update from 11/11/81 review.

* Added Clear-to-Send output.

1/7/82

* Revised I/O connector pin definition to reflect Attleboro plug definition.

1/28/82

* Revised PIO connector to reflect newly desired pin requirements.

* Revised signal definitions to include RDBEN* and W5, W6, W7, and W8.

* Added PAL definition.

2/5/82

* Added pictures for pin definitions on 25-pin D connector and 16-pin, pin header PIO connector.

SECTION 5

RS-232 ELECTRICAL DEFINITION

5.1 ORGANIZATION

The RS-232 PCB shall furnish two EIA RS-232C like ports, and a single 8-bit Bidirectional Port with one CRU IN and one CRU OUT bit for simple parallel operating devices. Deviations from the EIA RS-232C Specification lie mostly in the switching time area due to RFI considerations now imposed by the Federal Communications Commission.

5.2 GENERAL

* There shall be no more than one input connected to the System driven Bus. No more than three open collector or tri-state outputs may be connected to drive the System Bus. Both bus drivers and receivers shall be physically located close to the System I/O connector.

* Memory CRU space decodes shall comprehend PLA decoding as a cost reduction path.

* RS-232 level translators for line drivers shall conform to DWG WA0000MBJT.

* Adequate decoupling shall be provided on the logic and the RS-232 ports.

5.3 KNOWN 99/4A TO 99/4B SOFTWARE INCOMPATIBILITIES

* The baud rate generator in the TMS9902 UART is a divide by counter, and will require a different count for the 99/4A 3MHz clock than for the 2.66MHz 99/4B clock.

* Data from/to the 9902 UARTs is in the very slow access VDP RAM for the 99/4A. It will be in primary RAM for the 99/4B.

5.4 99/4A-99/4B DETERMINATION

Separate DSR ROMs shall be used for each system, and this device shall be socketed.

5.5 DESIGN VERIFICATION

Characterization with respect to System level propagation delays shall be performed on all of the QUAL units, and others as is required. If any negative deviations from design values are found, they shall drive any design changes required.

5.6 TEST CONSIDERATIONS

Signature Analysis shall be designed in as the primary fault isolation tool, and test specifications for this PCB shall be written after both design and prototype debug have been completed.

5.7 LED INDICATOR

A single LED shall be provided that is under Software Control. The LED shall be turned on every time the RS-232 port is utilized in order to blink the LED during normal operation. If self testing determines the PCB to be defective, the LED shall be left ON. It shall be turned ON during the self test operation, and then turned OFF if the PCB tests good.

5.8 PARALLEL PORT

The parallel port shall be configured as an 8-bit bidirectional data port with four CRU based handshake lines. The data port shall respond to any address in the upper 4K half of the DSR ROM space, and data OUT shall be latched. Data IN shall be gated directly to the System Data Bus. See the sections on the CRU definition and the Parallel I/O Port pin definition for additional information.

A single CRU OUT bit with an address bias of >4 shall be the handshake OUT bit, and a single CRU bit with an address bias of >4 shall be the handshake IN bit. Input/Output configuration shall be accomplished at an address bias of >2. A SBZ at that location shall configure the PIO Port as an OUTPUT Port, and a SBO shall cause it to function as an INPUT Port.

5.9 DSR ROM

The DSR ROM space decode shall be a function of the 19 System Address lines, MEMEN*, DBIN, and the signal PCBEN. PCBEN is a HIGH true signal that will be used in the Burn In Racks.

The DSR ROM shall be considered to be a 4K x 8 ROM, and shall be decoded to respond to the lower half of the DSR ROM space only. It shall also be connected such that an EPROM can be substituted with no wiring changes.

For the “first” RS-232 PCB, the DSR ROM base address shall be at >74000 (>4000 for Johnny Box), and the DSR ROM Page enable shall respond to a CRU base of >01300 (>1300 for the EXPN Box). For the “second” RS-232 PCB, the DSR ROM base address shall again be at >74000 (>4000 for EXPN Box), but the DSR ROM Page enable shall respond to a CRU base of >01500 (>1500 for the EXPN Box).

5.10 CRU DEFINITION

The CRU space shall comprehend 15 System Address Lines (the most significant three of the 99/4B shall be assumed to be zeros), MEMEN*, and the HIGH true signal PCBEN which will be used in the Burn In Racks. CRU addresses for the Johnny Boz are derived from 99/4B addresses by dropping the most significant character (3 bits).

5.10.1 First RS-232 PCB. The CRU base address for the “first” RS-232 PCB shall be at >01300, the DSR ROM Page enable shall respond to a CRU address of >01300, UART0 shall respond to a CRU base of >01340, and UART1 shall respond to a CRU base of >01380. A System RESET shall set the DSR ROM Page bit to a state that disables the DSR ROM.

5.10.2 Second RS-232 PCB. The CRU base address for the “second” RS-232 PCB shall be at >01500, the DSR ROM Page enable shall respond to a CRU address of >01500, UART0 shall respond to a CRU

base of >01540, and UART1 shall respond to a CRU base of >01580. A System RESET shall set the DSR ROM Page bit to a state that disables the DSR ROM.

5.10.3 LED Indicator Bit. A single bit shall be used to drive the Indicator LED. The power up sequence in the DSR ROM shall cause the LED to be set ON for the duration of the self test. If the PCB passes the self test operation, the LED shall be turned OFF. If a failure occurs, the LED shall be left ON. In addition, the LED shall be blinked with about a 200ms ON time to indicate RS232 PCB activity.

5.10.4 CRU Bit Definitions.

Output Bit Displacement	Definition
0	DSR ROM Page Enable, 1 = enabled
1	Parallel Port mode set, 1 = INPUT mode
2	Parallel Port Strobe bit
3	Spare Parallel Port bit
4	Flag 0
5	Clear to Send, RS232 Port 0, 0 = Active
6	Clear to Send, RS232 Port 1, 0 = Active
7	Indicator LED control, 1 = LED ON

Input Bit Displacement	Definition
0	Spare
1	Parallel Port configuration sense
2	Parallel Port Acknowledge sense bit
3	Spare Parallel Port sense bit
4	Flag 0
5	Clear to Send, RS232 Port 0 sense, 0 = Active
6	Clear to Send, RS232 Port 1 sense, 0 = Active
7	LED state sense

5.11 INTERRUPTS

The interrupts from both UARTs shall be “OR” connected, and drive Interrupt Level A (ILA). Interrupt Level Status Bits (ILSB) 0 and 1 shall be driven for UARTs 0 and 1 respectively for the “first” RS-232 and be used on the 99/4B, but the Johnny Box

shall not use interrupts. The ILSBs shall be gated to the Data Bus with the LOW true signal “SENILA”.

RS-232 #2 shall drive ILSBs 4 and 5 with UARTs 0 and 1 respectively, thus, ILSW bits shall be auto insert jumper options for both PCBs.

5.12 FLAGS

CRU bit 4 IN and OUT shall be connected to provide a Flag for S/W use.

5.13 I/O VOLTAGE LEVELS

All System Bus signals shall comply with standard TTL voltage levels, and all RS-232 I/O shall function with voltages bigger than 5V but less than 25V in absolute magnitude for the required RS-232 logic levels.

5.14 CONNECTORS

Both UARTs shall be connected to a single 25-pin D female connector, and shall conform to the pin definitions that are listed under RS-232 I/O PORT DEFINITION.

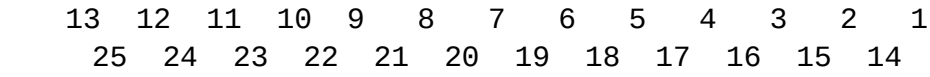
UART outputs shall drive translator output buffers, and UART inputs shall be driven by receiver translators.

RS232 I/O PORT DEFINITION

DATA SET PIN DEFINITIONS, FEMALE CONNECTOR

PIN #	TYPE	FUNCTION
1	driven	Protective Ground
2	received	Data to UART0
3	driven	Data from UART0
5	driven	Clear to Send CRU Out, U0
6	driven	1.8K Pull-up res to +12V
7	driven	Logic GROUND
8	driven	Data Carrier Detect UART0
12	driven	Data Carrier Detect UART1
13	driven	Clear to Send CRU Out, U1
14	received	Data to UART1
16	driven	Data from UART1
19	received	Data Terminal Ready UART1
20	received	Data Terminal Ready UART0

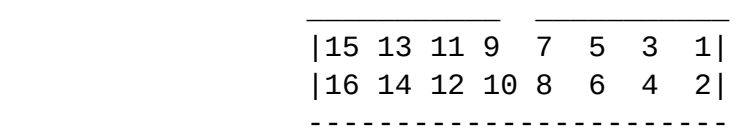
PIN VIEW OF 25-PIN D FEMALE CONNECTOR



PARALLEL I/O PORT DEFINITION

PIN#	FUNCTION
1	Handshake OUT
2	Data, LSB
3	Data
4	Data
5	Data
6	Data
7	Data
8	Data
9	Data, MSB
10	Handshake IN
11	Spare Input bit
12	1K Ohm Pull-up to +5V
13	10 Ohm Pull-up to +5V
14	Logic Ground
15	Spare Output bit
16	Logic Ground

PIN VIEW OF 16-PIN HEADER CONNECTOR



5.15 Y CABLE

A Y cable shall be available for users that wish to use both RS-232 ports. This cable shall be defined as follows:

PCB PIN	FUNCTION	P2 PIN	P3 PIN
1	Protective Ground	1	1
2	DATA to UART0	2	
3	DATA from UART0	3	
5	CTS CRU Out, U0	5	
6	1.8K P/U to +12V	6	6
7	Logic GROUND	7	7
8	DCD UART0	8	
12	DCD UART1		8
13	CTS CRU Out, U1		5
14	DATA to UART1		2
16	DATA from UART1		3
19	DTR UART1		20
20	DTR UART0	20	

System Bus I/O Connector Pin Definition
.100" PIN TO PIN SPACING, ATTLEBORO CONNECTOR

PIN #	MNEMONIC	FUNCTION
1		+5V 3-T Regulator supply voltage
2		+5V 3-T Regulator supply voltage
3	GND	Logic Ground
4		Not used, READY.A
5	GND	Logic Ground
6	RESET*	Active LOW System driven RESET
7	GND	Logic Ground
8		Not used, SCLK
9		Not used, BOOTPG*
10		Not used, AUDIO
11	RDBEN*	Active LOW Remote Data Bus Driver Enable control line
12	PCBEN	Active HIGH PCB enable for Burn In
13		Not used, HOLD*
14		Not used, IAQHDA
15	SENILA*	Interrupt Level A Sense Enable
16		Not used, SENILB*
17	INTA*	Active LOW Interrupt Level A
18		Not used, INTB*
19	D7	System DATA Bus, LSB
20	GND	Logic Ground
21	D5	System DATA Bus
22	D6	System DATA Bus
23	D3	System DATA Bus
24	D4	System DATA Bus
25	D1	System DATA Bus
26	D2	System DATA Bus
27	GND	Logic Ground
28	D0	System DATA Bus, MSB
29	A14.A	Address Bit
30	A15/COUT.A	Address Bit, LSB
31	A12.A	Address Bit
32	A13.A	Address Bit
33	A10.A	Address Bit
34	A11.A	Address Bit
35	A08.A	Address Bit
36	A09.A	Address Bit
37	A06.A	Address Bit
38	A07.A	Address Bit
39	A04.A	Address Bit
40	A05.A	Address Bit
41	A02.A	Address Bit
42	A03.A	Address Bit

PRODUCTION PCB PIN OUTS, CONTINUED

PIN #	MNEMONIC	FUNCTION
43	A00.A	Address Bit
44	A01.A	Address Bit
45	AMB.A	Address Bit
46	AMA.A	Address Bit
47	GND	Logic Ground
48	AMC.A	Address Bit, MSB
49	GND	Logic Ground
50	CLKOUT*	Active LOW CPU Clock
51	CRUCLK.A*	Active LOW CRU Output Clock
52	DBIN.A	Data bus Dir’tn HIGH is CPU READ
53	GND	Logic Ground
54	WE.A*	LOW true CPU Write Enable
55	CRUIN	HIGH true CRU Input Data
56	MEMEN.A*	Active LOW memory request
57		-12V 3-T Regulator supply voltage
58		-12V 3-T Regulator supply voltage
59		+12V 3-T Regulator supply voltage
60		+12V 3-T Regulator supply voltage

5.16 MNEMONIC DEFINITIONS

MNEMONIC	DEFINITION
AMC.A	System 19-bit Address Bus MSB
AMB.A	System 19-bit Address Bus
AMA.A	System 19-bit Address Bus
A00.A	System 19-bit Address Bus
A01.A	System 19-bit Address Bus
A02.A	System 19-bit Address Bus
A03.A	System 19-bit Address Bus
A04.A	System 19-bit Address Bus

MNEMONIC	DEFINITION
A05.A	System 19-bit Address Bus
A06.A	System 19-bit Address Bus
A07.A	System 19-bit Address Bus
A08.A	System 19-bit Address Bus
A09.A	System 19-bit Address Bus
A10.A	System 19-bit Address Bus
A11.A	System 19-bit Address Bus
A12.A	System 19-bit Address Bus
A13.A	System 19-bit Address Bus
A14.A	System 19-bit Address Bus
A15/COUT.A	System combination Address Bus LSB and CRU Output Data.
AMC.B	Buffered 19-bit Address Bus MSB
AMB.B	Buffered 19-bit Address Bus
AMA.B	Buffered 19-bit Address Bus
A00.B	Buffered 19-bit Address Bus
A01.B	Buffered 19-bit Address Bus
A02.B	Buffered 19-bit Address Bus
A03.B	Buffered 19-bit Address Bus
A04.B	Buffered 19-bit Address Bus
A05.B	Buffered 19-bit Address Bus
A06.B	Buffered 19-bit Address Bus
A07.B	Buffered 19-bit Address Bus

MNEMONIC	DEFINITION
A08.B	Buffered 19-bit Address Bus
A09.B	Buffered 19-bit Address Bus
A10.B	Buffered 19-bit Address Bus
A11.B	Buffered 19-bit Address Bus
A12.B	Buffered 19-bit Address Bus
A13.B	Buffered 19-bit Address Bus
A14.B	Buffered 19-bit Address Bus
A15/COUT.B	Buffered combination Address Bus LSB and CRU Output Data.
BDRVR*	Active LOW enable for the Data Bus Bidirectional Bus driver chip (SN74LS245)
CLKOUT.A*	Bus level System Clock. For 99/4 based systems it is the 3 MHz Phase 3 clock. For 99/4B based systems it is a 2.68 MHz clock similar to a 99/4A, but more than twice as wide and a different frequency.
CLKOUT.B*	Buffered System Clock. For 99/4 based systems it is the 3 MHz Phase 3 clock. For 99/4B based systems it is a 2.68 MHz clock similar to a 99/4A, but more than twice as wide and a different frequency.
CARDET0	UART0 Carrier Detect output.
CARDET1	UART0 Carrier Detect output.
CD0	RS-232 level Carrier Detect to 25-pin D Conn, pin 8.
CD1	RS-232 level Carrier Detect to 25-pin D Conn, pin 12.
CRUCLK.A*	System Level, Active LOW CRU Clock from the CPU.
CRUCLK.B	Buffered, Active HIGH CRU Clock from the CPU.
CRUCLK.B*	Buffered, Active LOW CRU Clock from the CPU.
CRUIN	HIGH True CRU data to the CPU (CRU READ Data).

MNEMONIC	DEFINITION
CRUO*	Active LOW enable for a bit CRU operation. It is the CRU base of either >1300 or >1500 for either module type (“First” or “Second” RS-232).
DATAIN0	RS-232 level received data from 25-pin D Conn, pin 2.
DATAIN1	RS-232 level received data from 25-pin D Conn, pin 14
DATAOUT0	RS-232 level data to 25-pin D Conn, pin 3.
DATAOUT1	RS-232 level data to 25-pin D Conn, pin 16.
DBIN.B	Buffered, Active LOW Data Bus Input control line. The data direction is from the PCB to the CPU when this line is HIGH.
DBIN.B*	Buffered, Active LOW Data Bus Input control line. The data direction is from the PCB to the CPU when this line is LOW.
DI0.A	Received Data for UART0.
DI1.A	Received Data for UART1.
DOUT0	UART0 data output.
DOUT1	UART1 data output.
DSRROM*	Active LOW DSR ROM enable to be ANDed with DBIN.B to drive the DSR ROM Chip Enable pin.
DTR0	RS-232 level Data Terminal Ready from 25-pin D Conn, pin 20.
DTR1	RS-232 level Data Terminal Ready from 25-pin D Conn, pin 19.
DTR0.A	Received Data Terminal Ready to UART0 Input.
DTR1.A	Received Data Terminal Ready to UART1 Input.
D0	System Side Data Bus MSB
D1	System Side Data Bus

MNEMONIC	DEFINITION
D2	System Side Data Bus
D3	System Side Data Bus
D4	System Side Data Bus
D5	System Side Data Bus
D6	System Side Data Bus
D7	System Side Data Bus LSB
FLAG0	Software Flag #0. Connects from a 259 output to a 251 input.
FLAG1	Software Flag #1. Connects from a 259 output to a 251 input.
FLAG2	Software Flag #2. Connects from a 259 output to a 251 input.
FLAG3	Software Flag #3. Connects from a 259 output to a 251 input, and also drives an indicator LED.
ILA*	Tristate, Active LOW driver for Interrupt Level A.
MEMEN.A*	System Memory Enable control signal from the CPU. When LOW it indicates that a memory access IS required by the CPU. When HIGH it indicates that a CRU MIGHT be taking place.
MEMEN.B*	Buffered Memory Enable control signal from the CPU. When LOW it indicates that a memory access IS required by the CPU. When HIGH it indicates that a CRU MIGHT be taking place.
PCBEN	Active HIGH PCB enable signal. It is used on the Burn In Rack to allow the controlling CPU to talk to only one PCB at a time. When LOW the PCB is disabled for both CRU and Memory operations.
PIO*	Active LOW enable for a Parallel I/O operation.

MNEMONIC	DEFINITION
PIOOC	Direction Control bit for the Parallel I/O Port. If LOW, the PIO Port shall function as an OUTPUT Port, and it will be LOW for either a Master Reset or a SBZ operation.
PIOR	Received handshake bit from Parallel I/O Port.
PIOS	Handshake bit for the Parallel I/O Port that is driven by the PCB. It will be LOW with either a SBZ or a Master Reset operation.
PIO0	Parallel I/O Data Port MSB
PIO1	Parallel I/O Data Port
PIO2	Parallel I/O Data Port
PIO3	Parallel I/O Data Port
PIO4	Parallel I/O Data Port
PIO5	Parallel I/O Data Port
PIO6	Parallel I/O Data Port
PIO7	Parallel I/O Data Port LSB
RD0	PCB Side Data Bus MSB
RD1	PCB Side Data Bus
RD2	PCB Side Data Bus
RD3	PCB Side Data Bus
RD4	PCB Side Data Bus
RD5	PCB Side Data Bus
RD6	PCB Side Data Bus
RD7	PCB Side Data Bus LSB
RDBEN*	Active LOW control line to enable remote Data Bus drivers at the 99/4 end of the connecting cable.

MNEMONIC	DEFINITION
RESET.A*	System Active LOW Master Reset line.
RESET.B*	Buffered Active LOW Master Reset line.
RPGEN	Active HIGH RS-232 DSR ROM Page Bit. It must be HIGH before the RS-232 DSR ROM may be accessed.
SENILA*	CPU driven line to allow the PCB to gate interrupt data to the system side of the Data Bus.
SI	Spare received handshake bit from Parallel I/O Port.
SO	Spare CRU handshake bit for the Parallel I/O Port that is similar to the signal PIOS.
UART0*	Active LOW chip select for the 9902 UART biased >40 from the CRU base.
UART1*	Active LOW chip select for the 9902 UART biased >80 from the CRU base.
U0INT*	UART0 interrupt drive.
U1INT*	UART1 interrupt drive.
WE.A*	System Write Enable from the CPU, and is used to Write data to the Parallel I/O Port.
WE.B*	Buffered Write Enable from the CPU, and is used to Write data to the Parallel I/O Port.
W5	Jumper wire to connect DTR0 to pin 20 on the 25-pin D Connector. W7 must not be connected if W5 is. W5 IS FACTORY INSERTED.
W7	Jumper wire to connect DTR0 to pin 11 on the 25-pin D Connector. W5 must not be connected if W7 is.
W6	Jumper wire to connect DTR1 to pin 19 on the 25-pin D Connector. W8 must not be connected if W6 is. W6 IS FACTORY INSERTED.
W8	Jumper wire to connect DTR1 to pin 18 on the 25-pin D Connector. W6 must not be connected if W8 is.

5.17 RS232 PAL12L6

```
DSRROM = V1*V2*A01*/A03*MEMEN*PCBEN

BDRVR = V1*V2*A01*MEMEN*PCBEN

PIO = V1*V2*A01*A03*MEMEN*PCBEN

CRUO = V2*/A01*A03*V3*/A05*A06*/A08*/A09*/MEMEN*PCBEN*/CCSEL
       + V2*/A01*A03*V3*A05*/A06*/A08*/A09*/MEMEN*PCBEN*CSSEL

UART0 = V2*/A01*A03*V3*/A05*A06*/A08*A09*/MEMEN*PCBEN*/CSSEL
        +V2*/A01*A03*V3*A05*/A06*/A08*A09*/MEMEN*PCBEN*CSSEL

UART1 = V2*/A01*A03*V3*/A05*A06*A08*/A09*/MEMEN*PCBEN*/CSSEL
        +V2*/A01*A03*V3*A05*/A06*A08*/A09*/MEMEN*PCBEN*CSSEL
```

1	V1	11	/MEMEN
2	/V2	12	PCBEN
3	A01	13	/DSRROM
4	A03	14	/BDRVR
5	/V3	15	/PIO
6	A05	16	/CRUO
7	A06	17	/UART0
8	A08	18	/UART1
9	A09	19	CSSEL
10	GROUND (POWER)	20	VCC (POWER)

P-CODE PCB, 99/4X AND JOHNNY BOX

SPEC DWG. #0000009

01/29/82

UPDATE TRACKS

First version written 7/28/81

8/17/81

* Added Mnemonic definitions.

8/18/81

* Added paragraph on software incompatibilities between 99/4A and 99/4X. There were none.

10/8/81

* Added DBIN and A05.B to the PLA equations for the GROM chip select.

* Added A05.B to the spare PLA input.

01/29/82

* Defined System I/O for Attleboro connector.

* Added RDBEN* signal definition.

* Added PAL definition.

* Deleted reference to the 75366 and used a 7417 instead.

* Added the LED with W1 and W2 wire jumpers.

SECTION 6

P-CODE ELECTRICAL DEFINITION

6.1 ORGANIZATION

The P-Code PCB shall be comprised of one (1) 4Kx8, and one (1) 8Kx8 Primary ROMs, and eight (8) GROM chips with the required decode logic to support them.

6.2 GENERAL

* There shall be no more than one input connected to the System driven bus. No more than three open collector or tri-state outputs may be connected to drive the System Bus. Both bus drivers and receivers shall be physically located close to the System I/O connector.

* Memory CRU space decodes shall comprehend PLA decoding as a cost reduction path.

* Required GROM voltage levels shall be designed in.

* Adequate decoupling shall be provided on the logic ROMs and the GROM chips.

6.3 KNOWN 99/4A AND 99/4X SOFTWARE INCOMPATIBILITIES

There are no known Software incompatibilities between the /4A and the /4X.

6.4 SOFTWARE REQUIREMENTS

It will be necessary to perform a “DUMMY” DATA READ from the GROM Library to initialize the GROM chips. This initialization insures the correct Address Counter byte is loaded on the first write to the Address Register.

6.5 DESIGN VERIFICATION

Characterization with respect to System level propagation delays shall be performed on all of the QUAL units and others as is required. If any negative deviations from design values are found, they shall drive any design changes required.

6.6 TEST CONSIDERATIONS

Signature Analysis shall be designed in as the primary fault isolation tool and test specifications for this PCB shall be written after both design and prototype debug have been completed. All ROMs and GROMs shall have CRC words in the last two byte locations.

Six spare CRU Output bits are available, and may be used in the testing process if practical.

6.7 DSR ROMs

The 8K DSR ROM space decode shall be a function of the 19 System Address lines, MEMEN*, DBIN, and the signal PCBEN. PCBEN is a HIGH true signal that will be used in the Burn In Racks.

The 4Kx8 DSR ROM shall be organized at >74C00 and the 8Kx8 ROM shall be based at >75000. The proper half of the 8Kx8 ROM shall be selectable with a CRU bit.

6.8 REMOTE DATA BUS DRIVER CONTROL

Provisions shall be made to drive the System bus line needed to control Data Bus drivers. This signal shall be driven active LOW any time the CPU is requesting a memory cycle from the P-Code PCB, and shall be open collector or equivalent.

6.9 GROMs

Eight GROM chips shall be parallel connected and addressed for chip select at >75BFC for a DATA READ, >75BFE for a ADDRESS READ, >75FFC for a DATA WRITE (not normally used) and >75FFE for an ADDRESS WRITE. DBIN shall be used to inhibit a READ at a WRITE address and vice versa.

6.10 CRU DEFINITION

The CRU space shall comprehend 15 System Address lines (the most significant three of the 99/4X shall be assumed to be zeros), MEMEN*, and the HIGH true signal PCBEN which will be used in the Burn In Racks. CRU addresses for the Johnny Box are derived from 99/4X addresses by dropping the most significant character (2 bits).

The CRU base address for the P-CODE PCB shall be >1F00, and a SBZ at >1F80 shall select the lower half of the 8Kx8 ROM to be based at >75000. A SBO at >1F80 shall select the upper half of the 8Kx8 ROM to be based at >75000. CRU displaced from both >1F00 and >1F80 by 1, 2, and 3 shall be connected to auto inserted wires, and used as test bits if practical.

An Indicator LED shall be jumper selectable between the DSR Page enable CRU bit (>1F00) and the CRU Output bit at >1F83. If W1 is inserted, a connection to >1F83 is made, and W2 makes connection to the DSR Page bit. A SBO instruction turns the LED ON, and a SBZ instruction turns it OFF. W2 is Factory inserted.

There shall be no CRU Input required.

6.10.1 CRU Bit Definitions.

Output Bit Displacement From >1F00	Definition
0	DSR ROM Page Enable, 1=enabled
1	Spare
2	Spare
3	Spare

Output Bit Displacement From >1F80	Definition
0	8Kx8 DSR ROM Half Select, 1=Upper, 0=Lower
1	Spare
2	Spare
3	LED, 1=ON, 0=OFF

6.11 System Bus I/O Connector Pin Definition

.100” PIN TO PIN SPACING, ATTLEBORO CONNECTOR

PIN #	MNEMONIC	FUNCTION
1		+5V 3-T Regulator supply voltage
2		+5V 3-T Regulator supply voltage
3	GND	Logic Ground
4	READY.A	System READY
5	GND	Logic Ground
6	RESET*	Active LOW System driven RESET
7	GND	Logic Ground
8		Not used, SCLK
9		Not used, BOOTPG*
10		Not used, AUDIO
11	RDBENA*	Active LOW Remote Data Bus Driver Enable control line
12	PCBEN	Active HIGH PCB enable for Burn In
13		Not used, HOLD*
14		Not used, IAQHDA
15	SENILA*	Interrupt Level A Sense Enable
16		Not used, SENILB*
17	INTA*	Active LOW Interrupt Level A
18		Not used, INTB*
19	D7	System DATA Bus, LSB
20	GND	Logic Ground
21	D5	System DATA Bus
22	D6	System DATA Bus
23	D3	System DATA Bus
24	D4	System DATA Bus
25	D1	System DATA Bus
26	D2	System DATA Bus
27	GND	Logic Ground
28	D0	System DATA Bus, MSB
29	A14.A	Address Bit
30	A15/COUT.A	Address Bit, LSB
31	A12.A	Address Bit
32	A13.A	Address Bit
33	A10.A	Address Bit
34	A11.A	Address Bit
35	A08.A	Address Bit
36	A09.A	Address Bit
37	A06.A	Address Bit

PRODUCTION PCB PIN OUTS, CONTINUED

PIN #	MNEMONIC	FUNCTION
38	A07.A	Address Bit
39	A04.A	Address Bit
40	A05.A	Address Bit
41	A02.A	Address Bit
42	A03.A	Address Bit
43	A00.A	Address Bit
44	A01.A	Address Bit
45	AMB.A	Address Bit
46	AMA.A	Address Bit
47	GND	Logic Ground
48	AMC.A	Address Bit, MSB
49	GND	Logic Ground
50	CLKOUT*	Active LOW CPU Clock
51	CRUCLK.A*	Active LOW CRU Output Clock
52	DBIN.A	Data bus Dir’tn HIGH is CPU READ
53	GND	Logic Ground
54	WE.A*	LOW true CPU Write Enable
55	CRUIN	HIGH true CRU Input Data
56	MEMEN.A*	Active LOW memory request
57		-12V 3-T Regulator supply voltage
58		-12V 3-T Regulator supply voltage
59		+12V 3-T Regulator supply voltage
60		+12V 3-T Regulator supply voltage

SECTION 7

P-CODE THEORY OF OPERATION

7.1 GENERAL DESCRIPTION

The P-Code PCB is a ROM/GROM based PCB to support the programming language PASCAL. It must be used on the system level in conjunction with a 32K or bigger Memory Expansion.

7.2 DSR ROMs

The 8K DSR ROM address space is comprised of a 4K ROM based at >74000, and an 8K ROM paged into two equal parts and based at >75000. A CRU bit located at >1F80 is used to select between the two halves, and a SBZ instruction at that address will select the lower half of the 8K ROM. Conversely, a SBO instruction at that same address will select the upper half. The DSR ROMs are shown on Page 5 of the P-CODE Schematics.

7.3 GROM ARRAY

An array of eight GROM chips gives a 48K Byte Graphics Read Only Memory, and the chips are all connected in parallel. Open collector drivers (SN7417N) and 470 Ohm pull-up resistors to +5V are used to interface the four PMOS GROM chip control lines to system, and a CMOS Bidirectional Data Bus Driver provides the proper HIGH logic level (+4.3V or higher) to the GROM data inputs. GROM Ground is connected to System Ground to prevent the internal P-CODE data bus from being driven below the System Ground level.

The GROM clock is derived from the System CPU clock, and has a frequency of 375 KHz that is derived from the System 3.0 MHz clock. This lower frequency was selected to provide higher GROM functional reliability.

The GROMs are accessed in the upper half of the DSR ROM space as follows:

* >75BFC for DATA READs

* >75BFE for ADDRESS READs

* >75FFC for DATA WRITEs (not a normal operation)

* >75FFE for ADDRESS WRITEs

This breaks down into:

AMC=AMB=AMA=1, A00=0, A01=1, A02=0, A03=A04=1, A05=X, A06=A07=A08=A09=A10=A11=A12=A13=1, A14=Data/Address Select, and A15/CRUOUT=X.

The System Level signal DBIN is used to determine a READ or a WRITE signal to the GROM chips as well as to inhibit a READ at one of the two WRITE addresses.

The GROM Array is shown on Page 4 of the P-CODE Schematics along with the divide by 8 counter (a 74LS161A) that is used to derive the GROM clock from the CPU clock. The TTL to MOS converters are also shown on that page.

7.4 PROGRAMMABLE LOGIC ARRAY

A PLA is used to generate all the chip selects, and it is supported by some combinational logic to generate terms that reduce the number of PLA inputs to an acceptable level (12 inputs or less).

It has been previously noted that the GROMs responded to four addresses in the upper DSR ROM space, and an 8-Input NAND gate is used to help trap those addresses. A09 is handled in the PLA in conjunction with this to provide the proper address trapping to disable the 8K DSR ROM and enable the GROMs. A pair of 4-Input AND gates and a single 2-Input OR gate are used to reduce the number of inputs required on the PLA. All of this logic is located on Page 1 of the P-CODE Schematics.

The following table is included to detail the operation of the PLA:

INPUT	8K ROM		4K ROM	BDBD	GROM		CRU OUT	SPARE
	+				+			
V1	H	H	H	H	H	H	X	X
V2	H	H	H	H	H	H	H	H
A01	H	H	H	H	H	H	L	L
A03	H	H	L	X	H	H	H	H
V3	X	X	X	X	X	X	H	H
A09	X	L	X	X	H	H	H	H
V4*	H	X	X	X	L	L	X	X
CRUCLK*	X	X	X	X	X	X	L	X
DBIN	H	H	H	X	H	L	X	X
MEMEN*	L	L	L	L	L	L	H	H
PCBEN	H	H	H	H	H	H	H	H
A05	X	X	X	X	L	H	X	X

“H” denotes a HIGH level, “L” a LOW level,
and “X” a Not Included value.
V1=AMCxAMBxAMAxPCPAGE, V2=A00x/A02*, V3=A04xA05xA06xA07,
V4*=A04xA06xA07xA08xA10xA11xA12xA13

7.4.1 MMI PAL12L6 Definition.

```
EKDSRCS = V1*V2*A01*A03*/V4*DBIN*MEMEN*PCBEN    ;  8K DSR ROM
        + V1*V2*A01*A03*/A09*DBIN*MEMEN*PCBEN
FKDSRCS = V1*V2*A01*/A03*DBIN*MEMEN*PCBEN       ;  4K DSR ROM
BDRVR   = V1*V2*A01*MEMEN*PCBEN      ;   BIDIRECTIONAL BUS DRIVER
GCS     = V1*V2*A01*A03*A09*V4*DBIN*MEMEN*PCBEN*/A05  ;   GROM CS
        + V1*V2*A01*A03*A09*V4*/DBIN*MEMEN*PCBEN*A05  ;   GROM CS
CRUWT   = V2*/A01*A03*V3*/A09*CRUCLK*/MEMEN*PCBEN  ;   CRU REG LD
SPAREO  = Spare output
```

1	V1	11	/MEMEN
2	/V2	12	PCBEN
3	A01	13	/EKDSRCS
4	A03	14	/FKDSRCS
5	V3	15	/BDRVR
6	A09	16	/GCS
7	/V4	17	/CRUWT
8	/CRUCLK	18	SPAREO
9	DBIN	19	A05
10	GROUND (POWER)	20	VCC (POWER)

7.5 SYSTEM READY CONTROL

The “READY” output of the GROM chips is connected to the input of a 74LS125AN bus driver, and the primary chip select (from the PLA) for the GROMs enables that particular driver (along with the GROMs). The output of the 125 is connected to the Tri-state driver System READY Status line to control the CPU, thus, when the GROM Array is enabled, the normally low GROM READY line causes the System to go “NOT READY”. When the last GROM chip goes “READY”, the System also goes READY. A fault (a screw up) in this area can hold the System “NOT READY” (lock the thing

up Tim). This logic is shown on Page 4 of the P-CODE Schematics.

A 5.6K pull-up on GROM READY was used to lighten the load on the READY output driver in the GROM chips.

7.6 CRU OUTPUT REGISTER

The CRU Output Register is shown on Page 1 of the P-CODE Schematics, and is connected such that 4-bit LDCR instructions can be utilized when operating at either >1F00 or >1F80.

7.7 ADDRESS AND DATA BUS BUFFERS

All System level signals are buffered prior to being used, and this logic is shown on Pages 2, 3, and 4 of the P-CODE Schematics.

7.8 SPECIAL CONSIDERATIONS

Spare –input OR gates are used for buffers to drive the SN7417 open collector drivers for the TTL/MOS interface, and the extra input to these gates is con the primary GROM chip select. In this manner transitions on the control lines in the GROM Array is limited to only those needed by the array, thus, System level noise is reduced.

7.9 POWER ANALYSIS

		+5mA		-5mA	
QUAN	DEVICE	MIN	MAX	MIN	MAX
1	SN7417N	29.0	41.0	-	-
1	SN74LS21N	1.7	3.4	-	-
1	SN74LS30N	.5	.8	-	-
1	SN74LS32N	4.9	9.8	-	-
1	SN74LS125AN	11.0	20.0	-	-
1	SN74LS161AN	19.0	32.0	-	-
3	SN74LS244N	81.0	138.0	-	-
1	SN74LS259N	22.0	36.0	-	-
1	PAL12L6	55.0	90.0	-	-
1	SN74LS245N	10.0	20.0 (est)	-	-
1	TMS4732N	65.0	95.0	-	-
1	TMS4764N	89.0	130.0	-	-
8	TMC0430N	64.0	80.0	64.0	80.0
Total Currents		452.1	696.0	64.0	80.0

7.10 MNEMONIC DEFINITIONS

MNEMONIC	DEFINITION
AMC.A	System Address Bus MSB
AMB.A	System Address Bus
AMA.A	System Address Bus
A00.A	System Address Bus
A01.A	System Address Bus
A02.A	System Address Bus
A03.A	System Address Bus
A04.A	System Address Bus
A05.A	System Address Bus
A06.A	System Address Bus
A07.A	System Address Bus
A08.A	System Address Bus
A09.A	System Address Bus
A10.A	System Address Bus
A11.A	System Address Bus
A12.A	System Address Bus
A13.A	System Address Bus
A14.A	System Address Bus
A15/COUT.A	System side combination Address Bus LSB and CRU Output Data.
AMC.B	Buffered Address Bus MSB
AMB.B	Buffered Address Bus

MNEMONIC	DEFINITION
AMA.B	Buffered Address Bus
A00.B	Buffered Address Bus
A01.B	Buffered Address Bus
A02.B	Buffered Address Bus
A03.B	Buffered Address Bus
A04.B	Buffered Address Bus
A05.B	Buffered Address Bus
A06.B	Buffered Address Bus
A07.B	Buffered Address Bus
A08.B	Buffered Address Bus
A09.B	Buffered Address Bus
A10.B	Buffered Address Bus
A11.B	Buffered Address Bus
A12.B	Buffered Address Bus
A13.B	Buffered Address Bus
A14.B	Buffered Address Bus
A15/COUT.B	Buffered combination Address Bus LSB and CRU Output Data.
A14.C	Buffered Address bit for higher logic “1” voltage for GROM array.
BDRVR*	Tristate enable for the Bidirectional Data Bus driver chip (SN74LS245).
CLKOUT.A*	System side of the System Clock. In 99/4A systems it is the 3 MHz Phase 3 clock, and in 99/4X systems it is a 2.68 MHz clock slightly more than twice the pulse width of 99/4A clock.

MNEMONIC	DEFINITION
CLKOUT.B*	Buffered side of the System Clock. In 99/4A systems it is the 3 MHz Phase 3 clock, and in 99/4X systems it is a 2.68 MHz clock slightly more than twice the pulse width of 99/4A clock.
CRUCLK.A*	Active LOW System side CRU Clock.
CRUCLK.B*	Buffered Active LOW CRU Clock.
CRULD*	Strobe for loading the CPU Out register.
DBIN.A	System side Data Bus direction indicator. A “0” indicates a WRITE to the PCB, and a “1” indicates a READ from the PCB to the CPU.
DBIN.B	Buffered Data Bus direction indicator. A “0” indicates a WRITE to the PCB, and a “1” indicates a READ from the PCB to the CPU.
DBIN.C	Buffered Data Bus direction indicator to gain the required higher logic “1” voltage for the GROM array.
D0	System Side of the Data Bus, MSB
D1	System Side of the Data Bus
D2	System Side of the Data Bus
D3	System Side of the Data Bus
D4	System Side of the Data Bus
D5	System Side of the Data Bus
D6	System Side of the Data Bus
D7	System Side of the Data Bus, LSB
EKDSRCS*	Chip Select signal for the 8K DSR ROM.
EKRPG	Half select for the 8K DSR ROM. A “0” on this line selects the lower half, and a “1” selects the upper half.

MNEMONIC	DEFINITION
FKDSRCS*	Chip Select signal for the 4K DSR ROM.
GCS*	Primary GROM chip select signal from the PLA. It must be buffered for more voltage drive before going to the GROM Array.
GCS.A*	Buffered GROM Chip Select to gain the higher logic “1” voltage required for the GROM Array.
GRDY	“READY” output from the GROM array.
MEMEN.A*	System side Memory Enable control signal. A “0” indicates that the CPU IS requesting a memory cycle, and a “1” indicates that the CPU MIGHT be requesting a CRU cycle.
MEMEN.B*	Buffered Memory Enable control signal. A “0” indicates that the CPU IS requesting a memory cycle, and a “1” indicates that the CPU MIGHT be requesting a CRU cycle.
PCBEN	Active HIGH control signal used in Burn In to enable the PCB to respond to either Memory or CRU accesses.
PCPAGE	P-CODE DSR ROM Page Bit. A “1” on this line enables The P-CODE DSR ROM, and a “0” disables it.
PD0	PCB side of the Data Bus, MSB
PD1	PCB side of the Data Bus
PD2	PCB side of the Data Bus
PD3	PCB side of the Data Bus
PD4	PCB side of the Data Bus
PD5	PCB side of the Data Bus
PD6	PCB side of the Data Bus
PD7	PCB side of the Data Bus, LSB
RDBEN*	Remote Data Bus Driver enable control line for use in 99/4-Exp Box Cable interface.

MNEMONIC	DEFINITION
READY.A	System READY input to CPU.
RESET.A*	System side of the Master Reset.
RESET.B*	Buffered Master Reset.
SPAREO*	Spare PLA output.
W1	Jumper wire used to connect >1F83 to the LED. If W1 is inserted, W2 shall not be.
W2	Jumper wire used to connect >1F00 to the LED. If W2 is inserted, W1 shall not be. W2 is Factory inserted.

7.11 P-CODE PAL12L6

```
EKDSRCS = V1*V2*A01*A03*/V4*DBIN*MEMEN*PCBEN    ;  8K DSR ROM

        + V1*V2*A01*A03*/A09*DBIN*MEMEN*PCBEN

FKDSRCS = V1*V2*A01*/A03*DBIN*MEMEN*PCBEN       ;  4K DSR ROM

BDRVR   = V1*V2*A01*MEMEN*PCBEN      ;   BIDIRECTIONAL BUS DRIVER

GCS     = V1*V2*A01*A03*A09*V4*DBIN*MEMEN*PCBEN*/A05  ;   GROM CS

        + V1*V2*A01*A03*A09*V4*/DBIN*MEMEN*PCBEN*A05  ;   GROM CS

CRUWT   = V2*/A01*A03*V3*/A09*CRUCLK*/MEMEN*PCBEN  ;   CRU REG LD

SPAREO  = Spare output
```

1	V1	11	/MEMEN
2	/V2	12	PCBEN
3	A01	13	/EKDSRCS
4	A03	14	/FKDSRCS
5	V3	15	/BDRVR
6	A09	16	/GCS
7	/V4	17	/CRUWT
8	/CRUCLK	18	SPAREO
9	DBIN	19	A05
10	GROUND (POWER)	20	VCC (POWER)

SECTION 8

EXPANSION BOX MEMORY EXPANSION

EXPANSION BOX 32K MEMORY EXPANSION
02/01/80

UPDATE TRACKS

8/24/81

* Added Section on testing.

8/25/81

* Added to Section on testing.

11/11/81

* Added paragraph on LED.

* Updated paragraphs on testing.

11/12/81

* Continued with general update from 11/11/81 review.

* Changed System I/O connector pinouts to comprehend 19 address lines.

1/28/82

* Added PAL to documentation.

* Changed System I/O pin definition to Attleboro plug connector.

* Added paragraph on Remote Data Bus Driver control.

1/29/82

* Revised device notation from alpha to Ui type.

02/01/82

* Added the 50mA LED load to the +5V current requirement.

8.1 MEU INTENT

The intent of this PCB is to provide functional equivalency to the existing 99/4 Memory Expansion Unit while functioning in the Exp. Box. The existing MEU will not function with a TMS9995 uP, and this unit shall not be so constrained also.

8.2 GENERAL

There shall be no more than one input connected to any System driven bus line, and bus buffers shall be located in close proximity of the I/O connector.

If 4116 DRAMs are to be used, one decoupling capacitor shall be provided for each DRAM on both the +12V and -5V buses in close proximity to the DRAM supply pins, and one 22 uF or bigger capacitor shall be provided on both the +12V and the -5V buses for each four DRAM chips. One bypass capacitor shall be included on the +5V bus for each four DRAM chips.

If 32K +5V only parts are to be used, each DRAM shall be bypassed, and two 22 uF or bigger capacitors shall be provided for the array. For either device type, .1 uF @ 50V Z5U axial lead devices shall be used.

Gridded GROUND lines shall be used through out the DRAM array where practical.

System RESET shall not be used on the Memory Expansion, but all sequential logic shall be either pulled up or down to allow initialization for testing on ATE.

The DRAMs shall function in the EARLY WRITE mode, and shall be timed by the Phase 3 System level clock.

Where practical, Signature Analysis hooks shall be included.

8.3 ADDRESS ORGANIZATION

The Memory Expansion PCB for the Exp Box shall be organized as a 32K x 8 DRAM located in the memory space in four equal segments. These are: 1) from >2000 thru >3FFF, 2) from >A000 thru >BFFF, 3) from >C000 thru >DFFF, and 4) from >E000 thru >FFFF.

8.4 MEMORY SPACE DECODE

The decode for the Memory space shall be a function of the 19 System Address lines and MEMEN*, and PCBEN. The last signal is an Active HIGH disable control signal that shall disable the ME PCB, and is for PCB Burn In use.

8.5 REFRESH

A Refresh READ shall be performed after every MEMEN* cycle regardless of what that particular memory cycle was for. If for some reason READY is held FALSE, a Refresh operation shall occur every 5 1/3 uS.

The Refresh Address Counter shall be configured such that one full 16K x 8 bank (i.e., 8 DRAM chips) is Refreshed before starting on the other bank. This address ordering is primarily for ease of Trouble Shoot and Repair.

8.6 DRAM ARRAY DRIVERS

Where practical, the buffers for the DRAM array shall be standard TTL rather than LS TTL. Series matching resistors shall be included to ease the capacitive loading effects of under and over shoot if long physical etch runs from the driver to the array are required.

8.7 REMOTE DATA BUS DRIVER CONTROL

Provisions shall be made to drive the System bus line required to enable the remote Data Bus drivers. This shall be a LOW true signal that is open-collector or equivalent.

8.8 LED

A LED shall be provided that is driven by a one-shot triggered by a CPU requested RAS. The period of the one-shot shall be 200mS +/-50%.

Error conditions on this card must be detected in S/W, and a S/W routine must keep accessing the MEU to keep the LED ON in case of a fail.

8.9 SYSTEM BUS PIN DEFINITION, (.1” CONNECTOR PIN SPACING)

.100” PIN TO PIN SPACING, ATTLEBORO CONNECTOR

PIN #	MNEMONIC	FUNCTION
1		+5V 3-T Regulator supply voltage
2		+5V 3-T Regulator supply voltage
3	GND	Logic Ground
4	READY.A	System READY
5	GND	Logic Ground
6		Not used, System RESET
7	GND	Logic Ground
8		Not used, SCLK
9		Not used, BOOTPG*
10		Not used, AUDIO
11	RDBENA*	Active LOW Remote Data Bus Driver Enable control line
12	PCBEN	Active HIGH PCB enable for Burn In
13		Not used, HOLD*
14		Not used, IAQHDA
15		Not used, SENILA*
16		Not used, SENILB*
17		Not used, INTA*
18		Not used, INTB*
19	D7	System DATA Bus, LSB
20	GND	Logic Ground
21	D5	System DATA Bus
22	D6	System DATA Bus
23	D3	System DATA Bus
24	D4	System DATA Bus
25	D1	System DATA Bus
26	D2	System DATA Bus
27	GND	Logic Ground
28	D0	System DATA Bus, MSB
29	A14.A	Address Bit
30	A15/COUT.A	Address Bit, LSB
31	A12.A	Address Bit
32	A13.A	Address Bit
33	A10.A	Address Bit
34	A11.A	Address Bit
35	A08.A	Address Bit
36	A09.A	Address Bit
37	A06.A	Address Bit

PRODUCTION PCB PIN OUTS, CONTINUED

PIN #	MNEMONIC	FUNCTION
38	A07.A	Address Bit
39	A04.A	Address Bit
40	A05.A	Address Bit
41	A02.A	Address Bit
42	A03.A	Address Bit
43	A00.A	Address Bit
44	A01.A	Address Bit
45	AMB.A	Address Bit
46	AMA.A	Address Bit
47	GND	Logic Ground
48	AMC.A	Address Bit, MSB
49	GND	Logic Ground
50	CLKOUT.A*	Active LOW CPU Clock
51	CRUCLK.A*	Active LOW CRU Output Clock
52	DBIN.A	Data bus Dir’tn HIGH is CPU READ
53	GND	Logic Ground
54	WE.A*	LOW true CPU Write Enable
55		Not used, CRUIN
56	MEMEN.A*	Active LOW memory request
57		-12V 3-T Regulator supply voltage
58		-12V 3-T Regulator supply voltage
59		+12V 3-T Regulator supply voltage
60		+12V 3-T Regulator supply voltage

SECTION 9

MEU TEST REQUIREMENTS

9.1 GENERAL TEST PHILOSOPHY

The intent of this Section is to detail the test plan for all stages of manufacture starting with Bare Etch Testing and ending with Burn In. The intent of testing is to insure top quality of the finished product; thus, test programs and test times shall be adjusted to complement the time available for testing during vital steps of the manufacturing process.

All active components on the Memory Expansion PCB shall be PEP III parts or equivalent.

9.2 GENERAL COMMENTS

* Each of the test systems described here shall have a RS-232 port implemented for Host to Satellite communications. This port is in addition to that for debug purposes.

9.3 BARE ETCH TESTING

The PCB shall be 100% Bare Etch Tested at Incoming QC. The result of this test shall be used to modify Production Line testing if desirable (for under etching it may be desirable to run more extensive tests at the first assembled PCB test station, etc.).

9.4 ASSEMBLED PCB TESTING

This test is intended for ATE testing (possibly on the HP3060A), and this is at a point in the line balance where a minimal test shall be run. PCB testing could possibly be done at this point on a functional test system that has the capability of

testing other PCBs in the 99/4 family since the load on the 3060A is an unknown at this time. The test patterns are defined in the next Paragraph.

9.4.1 Marching Patterns. This test shall not be included on the 3060A if it is used for pattern testing.

* Set the background (BKGND) to “0”s.

* Delay 400 mS.

* Starting with location 0 and advancing to the end of RAM sequentially, read, verify, and replace the BKGND Byte with all “1”s at each address location.

* Starting with the top end of memory and advancing sequentially to the lowest address, read, verify, and replace the BKGND Byte with all “0”s.

9.4.2 Checkerboard Pattern. The intent at this point is to verify that all cells respond to 1’s and 0’s; therefore, the checkerboard pattern is adequate.

* Starting with address = 0, sequentially load bytes with >55, >AA, >55, . . . to the end of the MEU address space. Delay 400 mS, and then verify that memory has not changed. Next, load >AA, >55, >AA, . . . into the MEU, delay 400 mS, and then verify that memory did not change.

9.4.3 Voltage Parametrics. The test interface shall provide LOW level voltages of .7V +15% -0%, and HIGH level voltages of 2.0V +5% -0%. Voltages from the ME PCB shall be sensed to be less than .4V +/-5% for a LOW, and bigger than 2.4V +/-5% for a HIGH level. All voltages are referenced from the ME PCB logic Ground at the System I/O connector.

Worst case parametric voltages shall not be run on the 3060A.

9.4.4 Power Supply Levels. Power supplied to the PCB shall be set at +7.0V for the +5V regulator, +14.5V for the +12V regulator, and -14.5V for the -5V regulator all referenced from the ME PCB logic Ground at the System I/O connector. Voltage check points shall be selected on the PCB at a point found by trial measuring on prototype PCBs to have the most voltage drop

for each level. Fail levels shall be 4.8V for the 5V supplies, and 11.5V for the +12V. Pass levels shall be bigger than or equal to 4.8V or less than or equal to 5.25V in magnitude for the 5V supplies, and bigger than or equal to 11.5V or less than or equal to 12.6V in magnitude for the +12V supplies. These trip levels shall be set with a DVM to +/-.05% of the magnitude listed.

The supply v0ltage set accuracies shall be +.1%, -0%.

9.5 BURN IN

The Burn In tests shall be the most comprehensive as an initial 96 hr Burn In time shall be used. There shall be a CPU PCB and a Controller PCB that drive 16 MEU PCBs per shelf in the Burn In Rack. Each CPU PCB shall be linked via a party line bus to a host machine for both the down loading of test programs and for data logging.

9.5.1 Test Patterns. A series of test patterns shall be used to adequately test address decoders and data paths, and are defined in the following paragraphs. At such time as is shown necessary, the pattern may be adjusted by adding new ones or by deleting existing ones. Note also that the TMS9900 moves WORDs rather than bytes, and the stored bit patterns will be word even with a MOVB instruction. An alternate pattern generator shall be provided.

9.5.1.1 GALPAT. A Galloping Pattern shall be used for sense amplifier and data path testing, and shall be as is described n this paragraph to test all manufacture’s devices. The procedure is as follows for an 8-bit wide memory chip array, and is to be run one time in each test sequence.

* Set the background (BKGND) of all 0’s.
* Write a Test Byte of 1’s in the first memory location.
* Delay 400 mS.
* Check that the Test Byte is still valid.
* Check that the first BKGND Byte is still valid.
* Check that the Test Byte is still valid.
* Check that the second BKGND Byte is still valid.

* Continue this alternating test of the Test Byte and the BKGND Byte until all BKGND Bytes have been tested.

* Restore the Test Byte to the value of the BKGND Byte, and put the Test Byte value in the next memory location past that previously tested.

* Perform the previously described procedure until ALL BKGND Bytes have been tested----not just those above the address of the Test Byte. Testing is continued until all address locations have contained the Test Byte.

* Set a BKGND of all 1's, use a Test Byte of all 0's, and run the complete test again.

9.5.1.2 Address Complementation. The following pattern shall be used to adequately test the address drivers, and shall be run as follows. Note that the concept must be translated to correspond to MEU PCB addressing of its disjoint space as this description pertains to the memory chip addressing. This test is to be run one time in each test sequence.

* Set a background (BKGND) of >FF, >00, >FF, >00, etc.

* Delay 400 mS.

* Verify address location 0 (the Base Address, and >FF should be found).

* Complement the address, and check that location (>00 should be found).

* Increment the Test Address, and check that location (>00 should be found).

* Complement the address, and check that location (>FF should be found).

* Reset the BKGND to >00, >FF, >00, >FF, etc.

* Rerun the tests as previously described, but with complemented data checks.

9.5.1.3 Sliding Diagonal. The Sliding Diagonal test writes test data into identical row and column numbers, and is as follows. Note that the RAM chip addresses must be translated into 99/4A addresses. Isn't it nice that so much thought was put into the

99/4A memory map? It has certainly made life miserable here! This test is to be run one time in each test sequence, and is to verify the memory for sensitivity to diagonal addressing.

* Set the background (BKGND) to “0”s.

* Delay 400 mS.

* Write a byte of >FF into ROW=COL=0.

* Check all other diagonal bytes, and finally the Test Byte.

* Set the Test Byte to 0, increment the ROW-COL number, store the Test Byte there, and continue as in the previous step until all diagonals have been checked.

* Set the BKGND to “1”s, and run the test again with the Test Byte = >00.

9.5.1.4 Random Address/Data Checks. This test sequence is to be run repetitively after the other tests have been run until the Host machine commands it to be halted.

* Set the background (BKGND) in location 0 of >5A.

* Generate address locations from a LSRG Counter with feedback bits of Qn and Qp. That seed word shall be >0001, and that shall be translated to the corresponding MEU PCB address. A separate LSRG Counter shall be used to generate data to be stored.

* Fill the MEU PCB with these bit patterns in that manner, and save the last LSRG address as a new address seed word, and the last data byte for that new seed byte.

* Delay 400 mS.

* Regenerate the random address/data information, and verify it for each memory location.

* Using the last LSRG Counter address as a new seed word, rerun the tests as outlined for that with a seed of >0001.

* Continue this self feeding test until told to stop by the host machine.

9.5.2 Power Cycling. It shall be the duty of the Host machine to Power Cycle each shelf of the Burn In Rack on a cycle of 30 minutes ON and 15 minutes OFF. This cycle shall be modified as additional information is obtained, and AC Line control shall be utilized rather than DC power control.

9.5.3 Error Data Logging. An eight position stack shall be assigned to each Burn In Rack PCB position for error data logging. Each position shall contain the type of test failed, the address of the failure, the test data, the faulty data, and the time into the test in hours and minutes. The latter information shall be used to adjust the Burn In time period.

SECTION 10

EXP BOX MEU THEORY OF OPERATION

10.1 PURPOSE

The purpose of this document is to detail the electrical operation of the 99/4 Exp Box Memory Expansion PCB.

10.2 APPROACH

The presentation of material will be to first cover 4116 DRAM fundamentals as they are used in the Memory Expansion PCB, and then to discuss the ME PCB functional blocks.

10.3 MEU SCHEMATIC SEGMENTATION

The schematics for the ME PCB are drawn on several B size sheets, and schematic page numbers are noted on Figure 1 for each functional block. The functional description of each schematic page is found at the bottom of that page.

10.4 TERMS USED

* BANK--8 DRAM chips to give 16K bytes, and all connected to the same RAS* and CAS* drivers.

* SEGMENT--an 8K contiguous DRAM space.

* PHASE 2 CLOCK--Mainframe Phase 2 clock. It does not come outside of the Mainframe, but most memory related control signals (WE* excepted) are timed with respect to this clock phase by the TMS9900.

* PHASE 3 CLOCK--Mainframe Phase 3 clock that is used in the Mainframe, and is available from the I/O Port for Peripheral use. The Memory Expansion PCB and other

peripherals use this clock.

10.5 TMS 4116 DRAM FUNDAMENTALS

10.5.1 GENERAL REMARKS. The fundamentals of DRAM operation revolve around eight main points: 1) RAS*, 2) CAS*, 3) the address bus, 4) W*, 5) supply current requirements, 6) DATA OUT--latched vs. unlatched, 7) DATA IN, and 8) REFRESH requirements. All will be discussed later in these notes.

A RANDOM ACCESS MEMORY has been corrupted to now mean a memory that can be either WRITTEN to or READ from, AND any memory location may be directly selected with equal ease by the ADDRESS lines to this memory unit. The latter part of this definition includes either a READ/WRITE or READ ONLY MEMORY, but the first part includes only a READ/WRITE memory. The first part is the corruption in the term RAM. Note also that ROM normally means Random Access Read Only Memory. . . so much for words though.

The TMS 4116 DRAM is of the address MUXed variety that has two chip select signals required to get the full address into the memory chip. The user of the chip must provide the external multiplexer to MUX the address bus, and the SN74LS257N quad 2/1 MUX is frequently used for this.

10.5.2 RAS* Most memories have an input that is used to tell the memory that an access request is required, or in other words, to turn the memory ON. RAS* is a LOW true signal that is used to load (strobe) the address on the DRAM Address Bus into the internal Row Address Register. RAS stands for Row Address Strobe. RAS* normally goes LOW before CAS* does.

10.5.3 CAS* CAS* is the Column Address Strobe, and is used to load to load the internal DRAM Column Address Register when CAS* goes LOW. It also enables the output buffer if a READ operation is indicated on the W* (READ/WRITE) control input (W*=1). CAS* will go LOW after RAS* does, and there is a minimum time period when both are active. Most designs (ME PCB included) require that they both go inactive at the same time when they are both active concurrently.

10.5.4 W* The W* input indicates a READ operation if W* is HIGH and a WRITE operation if W* is LOW. It must be stable very

shortly after CAS* occurs, but is not used on the falling edge of RAS*. If neither RAS* or CAS* is true, W* will not affect the DRAM if it changes state, and thus is quite often connected directly to the CPU signal DBIN.

10.5.5 SUPPLY CURRENT REQUIREMENTS. Current spikes typically 80 mA per chip on both the +12V and -5V supply lines occur when either RAS* or CAS* go LOW; that is, one 80 mA spike when RAS* goes LOW, and then another one when CAS* goes LOW. Bypass capacitors on each chip must furnish this abrupt but short term current requirement.

10.5.6 OUTPUT DATA. The TMS 4116 has unlatched data outputs that will release drive to the DATA BUS when CAS* returns to a high level. Many 4K DRAMs of the Address MUXed variety have latched outputs which do not behave in the previously described manner.

10.5.7 INPUT DATA. Input Data must be stable at the time that CAS* occurs. If HIGH Data is stored, HIGH Data will be read, and vice versa.

10.5.8 REFRESH. REFRESH is a term used to describe an operation required to reestablish data in each memory cell because they will otherwise be lost by capacitor discharge action. Either a READ or a WRITE to each of the 128 Row Addresses will accomplish this task, but since a WRITE operation would require one to know what should be in memory to begin with, a READ operation is normally used. All 128 combinations of the DRAM 7 bit Address Bus must be READ (Refreshed) within a 2 mS time period. At room temperature this may be a much longer time period, but it goes down as temperature increases.

There is no need to activate CAS* for this operation; thus, system level noise may be reduced by not driving CAS* for a REFRESH operation. The ME PCB design does not drive CAS* for a REFRESH operation.

10.6 CLOCKING SCHEME

The Phase 3 clock supplied from the CPU is the clock used in the ME PCB, and all clocking is done with either the TRUE Phase 3 or the FALSE Phase 3 clock to provide both Leading Edge (LE) and Trailing Edge (TE) clocking action. The period of the

clock is 333 nS, and the active pulse width is about 62 nS. From the TE of one clock to the LE of the next is about 270 nS(333-63)

10.7 ADDRESS SPACE

The ME PCB responds to two disjoint and unequal sized memory spaces in the 64K byte CPU memory space. The first is an 8K byte block starting at >2000 and ending with memory location >3FFF, and the second is a 24K byte block starting at >A000 and ending with >FFFF.

10.8 SYSTEM BUS BUFFERS

All output lines from the CPU are buffered before they are used on the ME PCB. The DATA Bus is also buffered prior to being used.

Input lines are unbuffered since a number of modules may drive them. Either open-collector or tri-state gates must be used to drive these lines. READY is an example of a line that may be either driven or sensed. The ME PCB senses this line for REFRESH purposes, but does not drive it.

10.8.1 Address Bus.

All Address bits are buffered.

10.8.2 Data Bus.

The Data Bus is buffered, and is only enabled for the ME PCB memory space.

10.8.3 Control Lines.

Five CONTROL lines are buffered for use on the ME PCB, and they are 1) MEMEN*, 2) DBIN, 3) PCBEN, 4) READY, and 5) PH3*.

10.9 DRAM SEGMENTATION

There are two banks of 8 each 4116 DRAMs to obtain the 32K byte capacity. Devices U20, U21, U22, U23, U24, U25, U26, and U28 respond to both the >2000 and the >A000 bases, and devices U28, U29, U30, U31, U32, U33, U34, and U35 respond to the >C000 and >E000 bases. Note that the address space between >A000 thru >FFFF is contiguous.

The Address Bit A1 functions as a bank select bit, and a pseudo address bit is formed by the ANDing of A0 and A2. This choice gives the proper four different combinations of the bank select and the pseudo address bits, and may be seen in the following table.

	A0	A1	A2	A3	A4-A7	A8-A11	A12-A15
>2000	0	0	1	0	0	0	0
>A000	1	0	1	0	0	0	0
>C000	1	1	0	0	0	0	0
>E000	1	1	1	0	0	0	0

The previous listing of A0, A1, A2, and A3 show that A2 is a “1” in 3 out of the 4 cases. It needed to be a “1” half of the time in one bank, and a “1” half of the time in the other bank for proper ME PCB operation. This condition is met by ANDing A0 and A2 to provide the modified address bit “APO”.

	APO	A1	A3	A4-A7	A8-A11	A12-A15
>2000	1	0	0	0	0	0
>A000	0	0	0	0	0	0
>C000	1	1	0	0	0	0
>E000	0	1	0	0	0	0

Notice here also that A1 is a “1” half of the time and a “0” the other half. This is the address bit used for 4116 bank selection with the pair of AND OR INVERT gates in A6.

10.10 ADDRESS MULTIPLEXER

A seven bit DRAM address is derived from either the 16 bit CPU Address Bus or the 8 bit Refresh counter buffers. A 2/1 MUX is used to obtain a 7 bit address from the CPU Address (3 CPU Address Bits are used to determine which of the four 8K segments will be selected, and note that this choice includes none of the four--MUX B2 does this). Devices U15 and U16 are 74LS257 MUXes with 3 state outputs, and are used for CPU address MUXing to the DRAM address bus. Seven 3 state drivers in U19 are used to MUX the Refresh Address on to the 7 bit DRAM Address Bus when the CPU Address Bus is not needed. Notice from Sheet 3 of the ME PCB Schematics that if the CPU is not requesting a MEU cycle, the DRAM Address Bus is connected to the Refresh Counter. This concept lowers the random system level noise generated by drivers unnecessarily driving large loads. This concept has also been applied to both the W* input of the 16 DRAM chip array and the DATA inputs as well.

10.11 REFRESH LOGIC

Refresh logic is found in devices U10, U18, U19, U7A, U12B, and U1. A Refresh Cycle will be initiated: 1) after every MEMEN* cycle of the CPU, 2) on 5 1/3 uS intervals if the CPU MEMEN* is inactive (HIGH), or 3) if CPU MEMEN* is active (LOW) AND “READY” to the CPU is FALSE (LOW). The latter case will occur when the CPU requests cycles from the Speech Module or possibly when the CPU accesses either GROMs or the VDP. This will give more than adequate margin on the required 2 mS Refresh time period. Each bank of 8 4116 DRAM chips is Refreshed individually (first one, and then the other).

U10 on Sheet 1 of the Schematics is a counter that is used to request Refresh cycles. It is put in the LOAD state to LOAD >E (14) into the counter when MEMEN* goes active LOW and READY stays HIGH. MEMEN* goes HIGH shortly after the Leading Edge (LE) of the Phase 2 clock in the 99/4 M/F, and A1 will be incremented to >F (15) on the TE of the very next Phase 3 clock. Now, the Ripple Carry output (pin 15) will go HIGH. U7A is connected to the Ripple Carry output of U10, will be clocked SET on the Leading Edge (LE) of the next Phase 3 clock pulse after U10 was incremented from >E to >F. U7A generates what is called REFRAS, and it will be set for 333 nS (one Phase 3 clock period). MEMEN* will be HIGH for at least 666 nS, and the Refresh operation will complete before MEMEN* can go LOW again.

If MEMEN* for some reason stays HIGH (CPU is executing a LDCR, STCR, MPY, or perhaps a DIV instruction), or if the CPU is accessing the Speech Module AND “READY” is LOW, U10 will count normally to >F, and a Refresh cycle will be initiated in the same manner just described. The Refresh Address Counter (A1) will be incremented on the TE of REFRAS.

10.12 RAS0/RAS1 SELECTION

Address bit A1 is synchronized to provide stability from one byte access into the next, and then used to select which of the two DRAM banks is to receive RAS*. The Refresh Address Counter MSB is used to select between the two banks for Refresh. This was done in order to completely REFRESH one bank before starting the other.

CAS* does not occur for Refresh cycles.

10.13 DATA CONNECTIONS

Both the data IN (D) and data OUT (G) pins on the 4116 DRAMs are connected together for EARLY WRITE operation.

10.13.1 Data TO DRAM.

WRITE data are gated to the DRAM banks through U3 (74LS245) which is enabled any time the ME PCB is selected.

10.13.2 Data FROM MEU.

READ data are gated to the System Data Bus by U3 (74LS245) with RAS* and CAS* both active (RAS*=CAS*=LOW); thus, data are stable for the 9900 CPU. See the attached timing diagrams in FIGURES 2 and 3 for this, and note that the 9900 takes READ data in during the Phase 1 clock time period. The proper Phase 1 is marked on the Timing Diagram.

10.14 TEST CONSIDERATIONS

A pull-down resistor is used to connect the HIGH true CLEAR inputs of the Refresh Address Counter (U18) to GROUND. This allows one to momentarily short this to +5V to reset the Refresh Address, or to disable the full Refresh Address space range. It is currently used to facilitate using Signature Analysis on the Refresh Logic.

A pull-up resistor is used on direct inputs to U7A, U9, U11, and U18 to allow Automatic Test Equipment (ATE) use on the ME PCB. The primary consideration is to allow the ATE to initialize the MEU logic to a known condition, and the signal is named INIT*.

10.15 EARLY WRITE

The Early Write technique is used to WRITE to the DRAMs. This simply means that W* is stable just before, and stays so all during the time when CAS* is active (LOW).

The System DBIN.A is clocked by G2 into FF U8B in order to guarantee its stability for the entire duration of the 4116 cycle. The FF is jammed to the RESET state when the 9900 is not requesting cycles from the ME PCB.

10.16 MEU OPERATION, GENERAL COMMENTS

This section is included to walk one memory cycle through. FIGURES 2 and 3 are timing diagrams of the system, and note that the CPU requires two bytes for its operation. If the CPU locates its Work Space in the MEU, quite often four bytes will be required, and six bytes will be required for a RTWP instruction. These multiple byte accesses will be “back to back” accesses running the MEU as fast as it will go (1 uS byte cycle times).

10.17 MEU IDLE STATE

A state counter made up of two SN74LS109A FFs (U11) is used to control the 4116 DRAMs. FF U9A is used to detect when the CPU is requesting ME PCB cycles, and is the control input to the state counter.

CAS is derived asynchronously after the address MUX has changed, and is the only case where asynchronous timing is used. There is no possible conflict, as it is timed directly off of an event that must occur before CAS* itself may occur.

10.18 FIRST CYCLE

The CPU will activate MEMEN* shortly after the LE of the Phase 2 clock in the Mainframe, and the Address Bus (and DATA Bus, too, if a WRITE operation is to occur) will be stabilized at that time, also. U1 is a PAL12L6 that is used to decode the CPU Address Bus and generate a cycle request if the MEU space is selected (it is also a function of the Burn In signal PCBEN). FF U9A is clocked OFF on the TE of PH3.B (with the PH3.B*), and the state counter will count from the 00 state (A2A=0 and A2B=0) to the state 01 (A2A=0, A2B=1) on the LE of the next PH3 clock (with PH3.B). U11B forms the signal Q2 that is the root signal of RAS*, and this signal is applied to the PAL12L6 to generate another RAS0* or RAS1* (the synchronized Address bit A1 selects which one). With the exception of the PAL which is found on Sheet 2 of the schematics, the aforementioned logic is found on Sheet 1.

When Q2 goes HIGH, the MUX control FF (U8A) is released from the jammed RESET condition, will be clocked SET with the TE of the same clock pulse that caused the state counter to be clocked to the 01 state. This delay provides more than adequate margin for RAS data hold time. Also, the cycle request sense FF U9A is jammed SET by Q2* for the duration of the DRAM cycle.

When the MUXing action has completed, a “0” will be gated to the Inverter C3E which in turn clocks on FF U7B to generate CAS. This signal then drives the DRAM array through a 27 Ohm resistor. The MUX control FF is also on Sheet 1, and the Address MUX with the CAS FF is on Sheet 3.

At this stage the DRAMs are turned on, and the cycle is initiated. The next PH3 LE will advance the state counter to the 11 state, and since RAS is a function of Q2, it is still LOW, (as is also CAS*). The 9900 will take data if a READ operation is to occur on the very next CPU PH1 clock, MEMEN* will return to a HIGH condition if the cycle is complete on the following CPU PH2 clock, and in any case the state counter will count back to the 00 state on the LE of the next PH3 clock pulse.

Once back in the 00 state both the MUX and CAS FFs are jammed RESET, RAS is turned OFF, and the cycle request sense FF U9A is once again able to detect if the CPU is asking (and it may still be) for a memory cycle.

10.19 CALCULATED POWER REQUIREMENTS

The total power requirements ignore 3-Terminal Regulator requirements, and the totals are based on a 1/3 duty cycle allocated to Operating, Refresh, and Idle modes of operation.

+12 Load mA		+5 Load mA		-5 Load mA	
TYP	MAX	TYP	MAX	TYP	MAX
---	---	---	---	---	---
103	175	319	515	373	2133

10.19.1 TTL Power Requirements. TTL currents were based on largest values taken with devices in their “normal” states; i.e., SN74LS245 and Refresh SN74LS241 in the tri-state condition, etc.

+12 Load mA		+5 Load mA		-5 Load mA	
TYP	MAX	TYP	MAX	TYP	MAX
---	---	---	---	---	---
0	0	368	564	0	0

10.19.2 MOS Power Requirements. MOS requirements are based on a 16 chip array, and single chip requirements are listed in the

following table.

	+12 Load mA		+5 Load mA		-5 Load mA	
	TYP	MAX	TYP	MAX	TYP	MAX
Operating	27	35	-	.1	50	200
Refresh	20	27	-	-	50	200
Stand By	.5	1.5	-	-	10	100

Further, assuming that the duty cycle will be 1/3 of each column, but for only eight chips (the other eight will be in the Stand By mode), the following array currents are obtained.

+12 Load mA		+5 Load mA		-5 Load mA	
TYP	MAX	TYP	MAX	TYP	MAX
103	175	-	1	373	2133

10.20 MEASURED POWER REQUIREMENTS

TO BE ADDED WHEN AVAILABLE

10.21 EXP BOX MEU PAL12L6 DEFINITION

```
RAS0   = MQ2*/A01S
         + REFRAS*/REFADR7

MESEL  = PCBEN*MEMEN*AMC*AMB*AMA*/A01*A02
         + PCBEN*MEMEN*AMC*AMB*AMA*A00*A01

RAS1*  = MQ2*A01S
         + REFRAS*REFADR7

         _______
AP02   = A00*A02

Spare Output

MEMENB = /MEMEN
```

1	PCBEN	11	REFADR
2	AMC	12	REFADR7
3	AMB	13	/RAS0
4	AMA	14	/MESEL
5	A00	15	/RAS1
6	A01	16	/AP02
7	A02	17	Spare Output
8	/MEMEN	18	/MEMENB
9	MQ2	19	A01S
10	GROUND (POWER)	20	VCC (POWER)

DOUBLE SIDED, SINGLE DENSITY DISK CONTROLLER PCB

SPEC DWG. #0000008

05/05/82

UPDATE TRACKS

8/18/81

* Added paragraph on 99/4A and 99/4B Software incompatibilities.

9/22/81

* Added CRU sense of Motor ON condition.

* Started Theory of Operation.

10/07/81

* Continued Theory of Operation.

01/29/82

* Changed System I/O definition to Attleboro plug.

* Added PAL definition.

02/02/82

* Continued general revision started 1/29/82.

05/05/82

* Fixed System Bus Pin screw up for interrupts, and added LCP and LINSP definitions.

SECTION 11

DS/SD DISK CONTROLLER ELECTRICAL SPECIFICATIONS

11.1 DISK CONTROLLER PCB (DOUBLE SIDED, SINGLE DENSITY)

The Disk Controller shall control up to three Double Sided, Single Density, 5 1/4" Mini Floppy disk drives through a Western Digital 1771 chip.

Memory addresses for the Johnny Box are derived by dropping the most significant character.

11.1.1 Intent. The intent of this PCB is to provide equivalency to the existing 99/4 Disk Controller Module while functioning in either the Johnny Box or the 99/4B. Two additional features shall be added in the form of a side select and a “drive connected” sense for each of the three possible drives.

11.2 GENERAL

* There shall be no more than one input connected to the System driven Bus. No more than three open collector or tri-state outputs may be connected to drive the System Bus.

* Memory/CRU space decodes shall comprehend PLA decoding as a cost reduction path.

* Timing considerations for the WD 1771 shall be made such that none are either violated or marginal.

* An adequate number of decoupling capacitors shall be provided for the logic chips. Particular attention shall be paid to MSI and LSI chips.

* RFI considerations shall be applied to the Drive I/O port.

* All System Bus signals driven by the Disk Controller shall

comply with standard TTL voltage levels.

11.3 KNOWN 99/4A AND 99/4B SOFTWARE INCOMPATIBILITIES

As of 8/18/81 there are no known incompatibilities.

11.4 TESTABILITY

Signature Analysis shall be designed in as the desired method of test, and test specifications shall be written for this PCB after both the design and debug efforts have been completed.

11.5 DESIGN VERIFICATION

System level propagation delays shall be carefully measured on each of the QUAL units and compared against design values. Any negative deviations shall be fully understood, and these shall drive redesign where required.

11.6 DSR ROM

The DSR ROM space decode shall be a function of the 18 System Address lines, MEMEN*, DBIN, the DSR ROM Page enable, and the signal PCBEN. PCBEN is a HIGH true signal that will be used in the Burn In Racks.

The DSR ROM shall be considered to be an 8Kx8 ROM (or a pair of 4Kx8 ROMs), and shall be connected such that an EPROM(s) can be substituted with no wiring changes. The 1771 shall occupy a trapped area in the top of the DSR ROM space. This area shall be defined by the AND combination of the following Address bits HIGH: AMC, AMB, AMA, A0*, A1, A2*, A3, A4, A5, A7, A8, A9, A10, and A11.

The DSR ROM base address shall be at >34000 (>4000 for Johnny Box), and the DSR ROM Page enable shall respond to a CRU base of >0110C (>110C for the Johnny Box).

11.7 CRU DEFINITION

The CRU space shall comprehend 15 System Address lines (the most significant two Address lines being ignored) and the HIGH true signal PCBEN which will be used in the Burn In Racks.

The CRU base address for the Disk Controller PCB shall be at >01100, and System RESET shall reset all output bits to a LOW value (same as SBZ at >01100 instruction).

11.7.1 CRU Output Bit Definitions.

DISPLACEMENT	FUNCTION
0	Disk DSR ROM Page Enable, 1=enabled Also used for LED, 0=OFF, 1=ON
1	Motor keep alive strobe, (pulse formed by a SBO 1 – SBZ 1 inst combination
2	Wait enable for 1771 chip communication 1=enabled
3	Head Load timing to 1771 chip, 1=load head
4	Drive #1 Select, 1=selected
5	Drive #2 Select, 1=selected
6	Drive #3 Select, 1=selected
7	Side Select, 0=Normal, 1=Opposite

11.7.2 CRU Input Bit Definition. The functions to be sensed through the CRU are the “HEAD LOAD” output of the WD 1771 chip, the three “drive connected” sense lines, and the Head Select line. These are detailed in the following table.

DISPLACEMENT	FUNCTION
0	HEAD LOAD output of WD1771 chip
1	“Drive #1 Connected” sense, 0=connected
2	“Drive #2 Connected” sense, 0=connected
3	“Drive #3 Connected” sense, 0=connected
4	Motor ON sense, 0=ON, 1=OFF
5	VCC
6	VCC
7	Ground

11.8 SYSTEM INTERFACE FOR WD 1771

Since the 1771 was designed to interface to an 8080 uP, special care shall be exercised in the timing area so as not to violate the required 1771 timing.

11.9 DATA/CLOCK SEPARATOR

An external Data/Clock separator shall be used instead of the 1771 internal separator. One shots shall be avoided if practical as a design goal.

11.10 MOTOR DRIVE KEEP ALIVE

A five second keep alive circuit shall control the disk drive motor line. The “keep alive” function shall be realized by pulsing the circuit (SBO/SBZ) from the CRU output.

11.11 WD 1771 CRYSTAL OSCILLATOR

A one MHz crystal controlled clock shall be provided for the 1771 chip.

11.12 INTERRUPTS

The Disk Controller PCB shall be connected to interrupt on ILB with an ILSB of bit 0.

11.13 CONNECTORS

There shall be a single 34-pin male PCB connector for external disk drive I/O and a single 34-pin header type connector for the internal drive. If used, the internal drive should be the first possible drive.

11.14 I/O CONNECTOR GROUND RETURNS

The odd pin numbers of the 34-pin I/O connectors are all Ground pins. They shall be bussed together into a bus of .125" width or bigger, and run as short as is practical to the Ground pins of the driver chips and then to the receiver chips. This shall be done in order to provide a good Ground return for RFI and other TTL considerations.

11.15 RECEIVER PULL-UP RESISTORS

All pull-ups on received I/O lines shall be 1K Ohms with the exception of the DATA line. It shall be pulled up with a 470 Ohm resistor.

11.16 I/O DRIVERS

Driven I/O to the disk drives shall be open collector devices capable of sinking 16 mA minimum.

11.17 I/O RFI CONSIDERATIONS

A LC pi filter network shall be used on I/O lines as necessary to provide acceptable RFI levels.

11.18 DISK DRIVE I/O PORT DEFINITION, BOTH PORTS

PIN	TYPE	FUNCTION
1		Logic GROUND
2		not used
3		Logic GROUND
4		not used
5		Logic GROUND
6		not used
7		Logic GROUND
8	recve	Index Pulse from Drive, LOW TRUE PULSE
9		Logic GROUND
10	drive	Drive Select #1, LOW=SELECTED
11		Logic GROUND
12	drive	Drive Select #2, LOW=SELECTED
13		Logic GROUND
14	drive	Drive Select #3, LOW=SELECTED
15		Logic GROUND
16	drive	Motor Control, LOW=ON
17		Logic GROUND
18	drive	Head Step Direction, LOW=STEP OUT
19		Logic GROUND
20	drive	Head Step Pulse, LOW TRUE FALSE
21		Logic GROUND
22	drive	Write Data, LOW=TRUE
23		Logic GROUND
24	drive	Write Gate, LOW=WRITE ENABLE
25		Logic GROUND
26	recve	Track 00, LOW=TRACK 00
27		Logic GROUND
28	recve	Write Protect, LOW=PROTECTED
29		Logic GROUND
30	recve	Read Data, LOW=TRUE
31		Logic GROUND
32	drive	Side Select, 0=Opposite, 1=Normal
33		Logic GROUND
34		not used

11.19 SYSTEM BUS PIN DEFINITION

.100” PIN TO PIN SPACING, ATTLEBORO CONNECTOR

PIN #	MNEMONIC	FUNCTION
1		+5V 3-T Regulator supply voltage
2		+5V 3-T Regulator supply voltage
3	GND	Logic Ground
4	READY.A	System READY
5	GND	Logic Ground
6	RESET*	Active LOW System driven RESET
7	GND	Logic Ground
8		Not used, SCLK
9		Not used, LCP
10		Not used, AUDIO
11	RDBEN*	Active LOW Remote Data Bus Driver Enable control line
12	PCBEN	Active HIGH PCB enable for Burn In
13		Not used, HOLD*
14		Not used, IAQHDA
15		Not used, SENILA*
16	SENILB*	Active LOW sense Interrupt Level B
17		Not used, INTA*
18	INTB*	Active LOW Interrupt Level B
19	D7	System DATA Bus, LSB
20	GND	Logic Ground
21	D5	System DATA Bus
22	D6	System DATA Bus
23	D3	System DATA Bus
24	D4	System DATA Bus
25	D1	System DATA Bus
26	D2	System DATA Bus
27	GND	Logic Ground
28	D0	System DATA Bus, MSB
29	A14.A	Address Bit
30	A15/COUT.A	Address Bit, LSB
31	A12.A	Address Bit
32	A13.A	Address Bit
33	A10.A	Address Bit
34	A11.A	Address Bit
35	A08.A	Address Bit
36	A09.A	Address Bit

PRODUCTION PCB PIN OUTS, CONTINUED

PIN #	MNEMONIC	FUNCTION
37	A06.A	Address Bit
38	A07.A	Address Bit
39	A04.A	Address Bit
40	A05.A	Address Bit
41	A02.A	Address Bit
42	A03.A	Address Bit
43	A00.A	Address Bit
44	A01.A	Address Bit
45	AMB.A	Address Bit
46	AMA.A	Address Bit
47	GND	Logic Ground
48	AMC.A	Address Bit, MSB
49	GND	Logic Ground
50	CLKOUT*	Active LOW CPU Clock
51	CRUCLK.A*	Active LOW CRU Output Clock
52	DBIN.A	Data bus Dir’tn HIGH is CPU READ
53	GND	Logic Ground
54	WE.A*	LOW true CPU Write Enable
55	CRUIN	HIGH true CRU Input data
56	MEMEN.A*	Active LOW memory request
57		-12V 3-T Regulator supply voltage
58		-12V 3-T Regulator supply voltage
59		+12V 3-T Regulator supply voltage
60		+12V 3-T Regulator supply voltage

SECTION 12

DISK CONTROLLER THEORY OF OPERATIONS

12.1 PURPOSE

The purpose of these notes is to provide a detailed Theory of Operation to aid in Trouble Shoot and Repair (TS&R). The intent of the Disk Controller PCB is to provide a unit very similar to the existing Disk Controller Module, but with minor enhancements. The date for the JAN CES Show dictated that we do very little development effort. We did add an 8-bit CRU Input port to replace the 1-bit one on the existing DCM, and designed the timing one-shots out of the Data/Clock Separator. We also added simple sense circuits to determine if a drive was connected to the desired drive number (a total of 3 sense circuits), and used the spare CRU Output bit to be a “side select” to allow double sided disks.

12.2 AREAS OF INTEREST

There are about 11 major areas of interest on this PCB, and will be covered in detail in the following paragraphs.

12.2.1 PLA and Support Logic. All major System Bus decoding is done in a Programmable Logic Array, and there are five out of the six available outputs used. Additional logic in the form of a 3-AND, an 8-NAND, and a 3-NOR is used to reduce the number of inputs required on the PLA. Additionally, the 8-NAND is used to determine when the upper DSR ROM (it responds starting at >75000) should be disabled, and the WD 1771 chip enabled in its place. This occurs at the top end of the upper DSR ROM space (starts with >75FF0).

The 3-AND gate ANDs the three most significant bits of the System Address Bus together in order to obtain a 3 to 1 PLA input reduction, and is used only for memory address decodes and not for CRU operations.

The 3-NOR gate is used only for CRU decodes and also gives a 3 to 1 PLA input pin reduction.

12.2.2 WD1771 Disk Controller Chip. The Chip select to the WD1771 chip is driven LOW when the WORD address space is satisfied. One uS later, the Read Enable input will be driven if DBIN is HIGH. If DBIN is LOW, the Write Enable input is driven with WE* a little longer than 1 uS later than the WD1771 Select. A15/COUT is the gating element in the first case, and both A15/COUT and WE* are gating elements in the second.

12.2.3 READY Control. The System READY line is manipulated only when data is being Written To or Read From the Disk Drive. This is enabled by a SBO 2 operation, and once done, any access of the WD1771 chip (if the Keep Alive One-shot has not timed out) will cause the System READY line to go LOW until either a Data Request (DRQ) or an Interrupt Request (IRQ) from the WD1771 occurs.

12.2.4 DSR ROMs. Two 4K*8 DSR ROMs are required for normal operation, but could just as easily have been a single 8Kx8 ROM. Neither of these ROMs can be accessed until the DSR page bit (at >1100) has been turned ON.

12.2.4.1 Low ROM. The Low DSR ROM is based at >4000, and is fully accessable between >4000 and >4FFF.

12.2.4.2 High ROM. The High DSR ROM is based at >5000, and has the upper 16 bytes trapped out (only 4 were needed) for the WD1771 chip.

12.2.4.3 WD1771 Trap. The WD1771 chip was not decoded all of the way down to the last four upper bytes because of the unavailability of two more NAND inputs.

12.2.5 Disk Drive Side Interface. The lines to the Drive are all driven with open collector power drivers, and the lines received from the drive are pulled up and then buffered with Schmidt trigger non-inverting gates. The Pull-up values are 1K Ohms except for the received data which is a 470 Ohm value.

12.2.6 CRU Output. An 8-bit 74LS259 Octal Latch is used for a CRU Output Register, and responds linearly to a CRU address of >1100. There are no spare output lines.

12.2.7 CRU In. A 74LS251 is used to provide an eight line CRU input interface. Two inputs are spares.

12.2.8 Bus Buffers. Bus Buffers are used for all lines received except for RESET.A* which drives only one unit load. With the exception of CRUIN, all lines to the System Bus are driven with line drivers. CRUIN is LS TTL driven, and the driver was located as close to the I/O pin as was practical.

12.2.9 Interrupts. The Disk Controller PCB interrupts on Level B, and is sensed on Data Bit 0.

12.2.10 Master Oscillator. An eight MHz Crystal controlled oscillator is used as a master oscillator and then divided by 8 to feed the WD1771 chip. The fundamental frequency was chosen to obtain a smaller crystal can size.

ATE provisions have been included to isolate the oscillator from the WD1771, and drive the WD1771 from a remote oscillator.

12.2.11 Data-Clock Separator. The fundamental purpose of the Data-Clock Separator is to separate the raw data stream from the Disk Drive into CLOCK pulses and DATA pulses. In accomplishing this function it must shape the raw data pulse width for the WD1771 chip, compensate for missing clock pulses, and resync to look for CLOCK pulses if too many DATA pulses occur (4) with no CLOCK pulses in between. Up to 3 missing CLOCK pulses can normally occur, thus some compensation for raw data stream switching is required.

The data rate for the Mini-Floppy Drive is 125KHz with FM DATA/CLOCK encoding, and this yields a CLOCK period of 8 uS. A 4 uS time displacement occurs between the leading edge (LE) of the CLOCK and the LE of the DATA pulse if one occurs.

12.2.11.1 Steering Logic. The steering logic consists of a SN74LS00 2-NAND gate that is connected to steer the Disk Data either to the WD1771 Clock or Data input. Gating is done such that the full pulse width must occur before it is possible to change from the clock output to the data output or vice versa. The logic is enabled by a One-shot that shapes the raw data from the drive to an approximate 500 nS pulse width for the WD1771 chip. Steering is accomplished with the control signal “STEER”. The control signal “STEER” is a “0” for the DATA path and a “1” for the CLOCK path.

12.2.11.2 Switching Logic. The purpose of the Switching Logic is to provide the control signal “STEER” to the 00 NAND gates in the Steering Logic. Raw disk data is steered to the data output if a clock output has occurred within the last 6 uS or if less

than four data outputs have occurred with no clock in between.

This logic is built around several 2-NAND gates, and a One-shot that is timed for 6 uS clock.

12.2.11.3 Missing Clock Compensation. Up to 3 missing CLOCK pulses will occur normally in the generation of the address mark, etc., in the header area preceding the actual data. Steering must be generated to switch over to the DATA path even though no CLOCK occurred to cause the switching to begin with. There will always be a DATA pulse (by definition) just prior to (4 uS) the missing clock. That DATA pulse is detected, and a pseudo CLOCK is later generated and fed to the switching logic (only) just as a separated CLOCK pulse normally is. This pseudo clock is inhibited if a normal CLOCK occurs, but would cause no ill effects if it were permitted. The pseudo clock is not fed to the CLOCK pulse path to the WD1771 chip.

If 4 CLOCK pulses are missing, the Missing Clock Compensation is inhibited, and the Switching Logic is set up to steer the very next raw data pulse to the CLOCK pulse line. A second One-shot timed for 5.4 uS and a DFF comprise this logic.

12.2.11.4 Missing Clock Counter. Still another missing clock function is required in the form of a Missing Clock Counter. This is for resynchronizing purposes if the separator accidentally sync’s to DATA rather than CLOCK pulses in the raw data stream. This incorrect sync can be caused by the “write splice” area between the header information and the data information, or in the area between sectors.

The Missing Clock Counter is INCREMENTED by separated DATA pulses and RESET by separated CLOCK pulses. If no separated CLOCK pulses occur between four separated DATA pulses, the counter “0” output is used to inhibit the Missing Clock Compensator from providing the pseudo CLOCK pulse to the Switching Logic. Three DFFs are used to count the steered raw data pulses to the Data output.

12.3 DSSD DISK PAL12L6

LOROM = V1*/A00*A01*/A02*/A03*DSKPG*MEMEN*PCBEN

HIROM = V1*/A00*A01*/A02*A03*V3*DSKPG*MEMEN*PCBEN

BDRVR = V1*/A00*A01*/A02*DSKPG*MEMEN*PCBEN

WDEN = V1*/A00*A01*/A02*A03*/V3*DSKPG*MEMEN*PCBEN

CRU   = /A00*/A01*/A02*A03*A07*V2*MEMEN*PCBEN

Spare Output

1	V1	11	VCC (LOGIC)
2	A00	12	V2
3	A01	13	/LOROM
4	A02	14	/HIROM
5	A03	15	/BDRVR
6	DSKPG	16	/WDEN
7	A07	17	/CRU
8	/MEMEN	18	Spare Output
9	PCBEN	19	V3
10	GROUND (POWER)	20	VCC (POWER)

12.4 MNEMONIC DEFINITIONS

MNEMONIC	DEFINITION
AMC.A	System 19-bit Address Bus MSB
AMB.A	System 19-bit Address Bus
AMA.A	System 19-bit Address Bus
A00.A	System 19-bit Address Bus
A01.A	System 19-bit Address Bus
A02.A	System 19-bit Address Bus
A03.A	System 19-bit Address Bus
A04.A	System 19-bit Address Bus
A05.A	System 19-bit Address Bus
A06.A	System 19-bit Address Bus
A07.A	System 19-bit Address Bus
A08.A	System 19-bit Address Bus
A09.A	System 19-bit Address Bus
A10.A	System 19-bit Address Bus
A11.A	System 19-bit Address Bus
A12.A	System 19-bit Address Bus
A13.A	System 19-bit Address Bus
A14.A	System 19-bit Address Bus
A15/COUT.A	System combination 19-bit Address Bus LSB and CRU Output Data.
AMC.B	Buffered 19-bit Address Bus MSB

MNEMONIC	DEFINITION
AMB.B	Buffered 19-bit Address Bus
AMA.B	Buffered 19-bit Address Bus
A00.B	Buffered 19-bit Address Bus
A01.B	Buffered 19-bit Address Bus
A02.B	Buffered 19-bit Address Bus
A03.B	Buffered 19-bit Address Bus
A04.B	Buffered 19-bit Address Bus
A05.B	Buffered 19-bit Address Bus
A06.B	Buffered 19-bit Address Bus
A07.B	Buffered 19-bit Address Bus
A08.B	Buffered 19-bit Address Bus
A09.B	Buffered 19-bit Address Bus
A10.B	Buffered 19-bit Address Bus
A11.B	Buffered 19-bit Address Bus
A12.B	Buffered 19-bit Address Bus
A13.B	Buffered 19-bit Address Bus
A14.B	Buffered 19-bit Address Bus
A15/COUT.B	Buffered combination 19-bit Address Bus LSB and CRU Output Data.
BDRVR*	Active LOW enable for the Data Bus Bidirectional Bus Driver Chip (SN74LS245).
CLK	Separated clock to WD1771 chip.
CLKOUT.A*	Bus level System Clock. For 99/4A based systems it is the 3 MHz Phase 3 clock.

MNEMONIC	DEFINITION
CLKOUT.B*	Buffered System Clock. For 99/4A based systems it is the 3 MHz Phase 3 clock.
CRUCLK.A*	System Level, Active LOW CRU Clock from the CPU.
CRUCLK.B*	Buffered, Active LOW CRU Clock from the CPU.
CRUEN*	Active LOW Disk SCR space enable.
CRUIN	HIGH True CRU data to the CPU (CRU READ Data).
CRURQST*	Active LOW CRU Output Register strobe. It is the negative AND of CRUEN* and CRUCLK.B*.
DBIN.A	Buffered Active HIGH Data Bus Input control line. The gate direction is from the PCB to the CPU when this line is high.
DBIN.B	Buffered Active HIGH Data Bus Input control line. The gate direction is from the PCB to the CPU when this line is high.
DDB0	PCB Side Data Bus, MSB
DDB1	PCB Side Data Bus
DDB2	PCB Side Data Bus
DDB3	PCB Side Data Bus
DDB4	PCB Side Data Bus
DDB5	PCB Side Data Bus
DDB6	PCB Side Data Bus
DDB7	PCB Side Data Bus, LSB
DIR	Head step direction from WD1771 chip.
DIR*	Buffered Head step direction to drive.
DRESET*	Reset line for the Disk Drive PCB. It is the OR of the System level Reset and the PCB Power-Up Reset.

MNEMONIC	DEFINITION
DRQ	Active HIGH Data Request from the WD1771 chip.
DSEL1	Drive #1 select from the CRU Output register.
DSEL2	Drive #2 select from the CRU Output register.
DSEL3	Drive #3 select from the CRU Output register.
DSKPGENA	Active HIGH page enable for the DSR ROMs.
DS1*	Buffered Drive Select to Disk Drive #1.
DS2*	Buffered Drive Select to Disk Drive #2.
DS3*	Buffered Drive Select to Disk Drive #3.
DTA	Separated data to WD1771 chip.
DVENA	Q output of the “Keep Alive” One-shot.
DVENA*	Q* output of the “Keep Alive” One-shot.
D0	System Side Data Bus MSB
D1	System Side Data Bus
D2	System Side Data Bus
D3	System Side Data Bus
D4	System Side Data Bus
D5	System Side Data Bus
D6	System Side Data Bus
D7	System Side Data Bus LSB
D10*	Active LOW sense for Drive #1 connected. It does not indicate that the drive motor is on.
D20*	Active LOW sense for Drive #2 connected. It does not indicate that the drive motor is on.

MNEMONIC	DEFINITION
D30*	Active LOW sense for Drive #3 connected. It does not indicate that the drive motor is on.
HIROMEN*	Enable for the DSR ROM that starts at >5000. The Chip Enables for the WD1771 are trapped out of the top end of this space; thus the CRCs cannot be read after the ROMs have been installed on the PCB.
HLT	Head Load Timing from the CRU Output Register to the WD1771.
HLD	Head Load output of the WD1771.
INTB*	Active LOW Interrupt Level B request.
INTRQ	Active HIGH Interrupt Request output of the WD1771.
IXP*	Active LOW Index pulse from the Drive.
IXP.A*	Buffered Active LOW Index pulse from the Drive.
KACLK	Keep Alive One-shot Clock from the CRU Output Reg.
LOROMEN*	Active LOW chip enable for the DSR ROM based at >4000.
MEMEN.A*	System Memory Enable control signal from the CPU. When LOW it indicates that a memory access IS required by the CPU. When HIGH it indicates that a CRU MIGHT be taking place.
MEMEN.B*	Buffered Memory Enable control signal from the CPU. When LOW it indicates that a memory access IS required by the CPU. When HIGH it indicates that a CRU MIGHT be taking place.
MTRON*	Active LOW Motor ON to Disk Drive.
OMHCK	Crystal controlled one MHz clock to WD1771 chip.

MNEMONIC	DEFINITION
PCBEN	Active HIGH PCB enable signal. It is used on the Burn In Rack to allow the controlling CPU to talk to only one PCB at a time. When LOW the PCB is disabled for both CRU and Memory operations.
RDBENA*	Active LOW enable for the System Data Bus Drivers on the 99/4 end of the interface cable.
RDDTA*	Complement Received Data from the Disk Drive.
READY.A	Active HIGH System Ready.
RESET.A*	System Active LOW Master Reset line from the CPU.
SENILB*	CPU driven line to allow the PCB to gate interrupt data to the system side of the Data Bus.
SIDSEL	Active HIGH Side select from the CRU Output Reg. A 0 selects the first (same as Single Side) side, and a 1 selects the second side. Either a RESET or a SBZ 7 operation will select the first side, and a SBO 7 operation is require to select the second side.
SIDSEL*	Active LOW Side select to the Drive. A 0 selects the second side, and a 1 selects the first side. Either a RESET or a SBZ 7 selects the first side, and a SBO 7 will select the second.
SRDTA	This is the Q output of a One-shot used to provide the correct Read Data pulse width for the WD1771 once the Data and Clock are separated.
STEP	Active HIGH output from the WD1771 chip to tell the Drive to step to another track. “DIR” tells which direction to step.
STEP*	Buffered “step” control line to the Disk Drive.

MNEMONIC	DEFINITION
ALB TK00*	Track 00 status signal from the Disk Drive.
ALB TK00*	Buffered Track 00 status signal from the Disk Drive.
WAITEN	CRU Output to enable Wait Reads and Wait Writes. Both are used to get data from and to the Disk Drive respectively.
WDRE*	Active LOW Read Enable to the WD1771 chip.
WDSEL*	Active LOW WD1771 memory space decode.
WDWE*	Active LOW Write Enable to the WD1771.
WE.A*	System Write Enable from the CPU, and is used to Write data to the Parallel I/O Port.
WE.B*	Buffered Write Enable from the CPU, and is used to Write data to the Parallel I/O Port.
WRTGT*	Active LOW Write Gate to the Drive.
WTDATA	WD1771 HIGH True data output to the Disk Drive.
WTDATA*	Buffered LOW True data to the Disk Drive.
WTG	Write Gate output of the WD1771.
WTPT*	Active LOW Write Protect status from the Drive. A LOW level is Write Protected.
WTPT.A*	Buffered Active LOW Write Protect status from the Disk Drive.

SECTION 13

SPEECH SYNTHESIZER THEORY OF OPERATION

13.1 PRINCIPLE OF OPERATION

The Speech Synthesizer generates synthetic speech within the synthesizer I.C. (TMC0285) from coded data stored in Phrase ROMs (PHROMS). The 0285 interfaces to the Home Computer through the Data Bus. I/O to the speech peripheral is enabled when SPEECH BLOCK ENABLE signal from the console is a logic HIGH. The 0285 in turn controls the PHROMS to fetch data when required. Data brought to the 0285 is fed to the speech synthesis network, there assembled into a digital code, then fed to a Digital to Analog Converter to generate the analog speech waveforms. The analog output is coupled back to the console sound I.C. and amplified to drive a speaker.

13.2 TMC 0285

The TMC 0285 (U1) is a MOS LSI circuit that contains not only data and control interface, but also complex circuitry that uses coded data strings obtained from the PHROMS to control a digital filter network. This filter network may be thought of as an electronic model of the human larynx. Output from the 0285 is an analog speech signal which requires no further processing other than amplification to drive a speaker. For a detailed explanation of the 0285, refer to TI Drawing # 1501640 and ELECTRONICS, August 31, 1978, page 109, "Three Chip System Synthesizes Human Speech."

13.3 TMC 0350 PHROMS

The PHROMS are TMC 0350 16K X 8 ROMS. The PHROMS use an 18 bit address of which the 4 MSBs select 1-of-16 PHROMS, although only two are installed in the Speech Synthesizer peripheral. It will be noted that since only four address lines are available on the 0350 ROM, several address cycles are required to fully address the ROM.

13.4 OPERATION

Activity in the speech peripheral is initiated by the Home Computer CPU through a Speech Select (SBE). The Speech Select signal is decoded in the console at address >9000 (READ) and >9400 (WRITE) and presented to the Speech Synthesizer as a single control line (SBE) on pin 2 of the I/O port. It is then necessary to redivide the SBE signal into a read and write select. The Read Select (RS) to the 0285 is decoded through U3 (LS138) from SBE, *A5, and *A5 (>9000). A Write Select (WS) is derived from SBE, A5, and A15 (>9400). These control signals determine whether the 0285 will put information on the Data Bus or receive information from the Data Bus. Immediately after a *RS or *WS the 0285 will take the system not ready by making READY at the I/O port a logic LOW. The Speech Synthesizer will hold the system not ready until the data being received has been latched in (WRITE) or the data being sent is stable on the bus (READ). The not ready time is around 20 microseconds but is variable and depends on which mode has been selected and the command. Timing can be obtained from the Speech Module Specification # 1034759.

After receiving a command, the 0285 begins processing and if required sends control and address to the PHROM. The control signals I0 and I1, pins 15 and 16 respectively, operate as follows:

I1	I0	Function
0	1	data read
1	0	address load
1	1	read and branch (not used in present system)

Address information is passed to the PHROMS on the ADD 1, 2, 4, and 8 lines, pins 2, 25, 23, and 21 respectively. The ADD1 is the LSB and ADD8 the MSB of the address nibble from the Data Bus D7 through D4. Data from the PHROMS is transferred to the 0285 serially over the ADD8 line following a READ function. Transfers are synchronized by the 160 KHz ROM Clock (U1-3).

The ROM Clock is a divide-by-four of the internal oscillator (U1-6). The oscillator is adjusted to 160 KHz by clipping R5, R6, or both out of the circuit. The speech output is open drain and requires a DC path to ground (R3) to operate. R3 sets an operating point at about one-third supply to prevent clipping the peaks of the audio output. Capacitor C2 provides DC

isolation and C6 along with R3 forma a low pass filter to trap noise from the 8 KHz sampling rate.

A sample sequence to speak a word assuming its address in PHROM has previously been obtained would be as follows:

The address is set to >9000 (speech write) by the console, SBE goes HIGH, *WS at U1 goes LOW, and READY (I/O pin 12) goes LOW taking the console not ready. Along with the address, the Data Bus information will contain a command code on D1 – D3 to LOAD ADDRESS. The format is as follows:

D0	D1	D2	D3	D4	D5	D6	D7
X	1	0	0	MSB			LSB

COMMAND CODE ADDRESS NIBBLE

The nibble of address and an I1 pulse would in turn be sent to the PHROMS. Upon completion of latching in the data, U1 releases the READY line and allows the console to continue. Since the PHROM takes 18 bits to fully address, four more LOAD ADDRESS commands are needed. This causes I1 pulses to be sent in sets of five.

With the address written the next command is a SPEAK. This follows a write-to-speech sequence as previously described. The command code for speak is D1=1, D2=0, D3=1, all other data lines are don't care states. The READY release is again completed when the data has been latched. The TMC 0285 will then issue a read pulse (I0) to the PHROM and a byte of data will be read in serially through U2-21 (ADD8). The TMC 0285 will continue to send I0 pulses as required to supply the data necessary to speak the word until a stop code is encountered. Speech activity will then stop until the next command is written to the speech module. During speech the audio waveform may be observed by looking at U1-8, note that I/O pin 44 is a low impedance across which little AC voltage will be observed.

If it is unknown to the CPU what the speech module is doing, its status can be read. This is accomplished by issuing a speech read, address >9400. The TMC 0285 will take the READY line LOW and set up the status on the Data Bus. When the data is stable, READY will be released and the status can be read. Status bits are interpreted as follows: D0=Talk Status (TS), D1=Buffer Low (BL), and D2=Buffer Empty (BE), all Active HIGH

signals. The BL and BE signals are used when inputting data on the Data Bus.

Other commands include READ BYTE, used to bring data from the PHROMS to the Data Bus, SPEAK EXTERNAL, used to put speech data into the TMC 0285 via the Data Bus, NOP, RESET, and READ AND BRANCH. For further information, refer to the previously cited documents.